DRAFT

MPX 110

24 bit

Dual Channel Processor

Service
Manual

Lexicon

Precautions

Save these instructions for later use.

Follow all instructions and warnings marked on the unit.

Always use with the correct line voltage. Refer to the manufacturers operating instructions for power requirements. Be advised that different operating voltages may require the use of a different line cord and/or attachment plug.

Do not install the unit in an unventilated rack, or directly above heat producing equipment such as power amplifiers. Observe the maximum ambient operating temperature listed in the product specification.

Slots and openings on the case are provided for ventilation; to ensure reliable operation and prevent it from overheating, these openings must not be blocked or covered. Never push objects of any kind through any of the ventilation slots. Never spill a liquid of any kind on the unit.

This product is equipped with a 3-wire grounding type plug. This is a safety feature and should not be defeated.

Never attach audio power amplifier outputs directly to any of the unit's connectors.

To prevent shock or fire hazard, do not expose the unit to rain or moisture, or operate it where it will be exposed to water.

Do not attempt to operate the unit if it has been dropped, damaged, exposed to liquids, or if it exhibits a distinct change in performance indicating the need for service.

This unit should only be opened by qualified service personnel. Removing covers will expose you to hazardous voltages.

 This triangle, which appears on your component, alerts you to the presence of uninsulated, dangerous voltage inside the enclosure… voltage that may be sufficient to constitute a risk of shock.

CAUTION

RISK OF ELECTRIC SHOCK
DO NOT OPEN

 This triangle, which appears on your component, alerts you to important operating and maintenance Instructions in this accompanying literature.

Notice

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications of Part 15 of FCC Rules, which are designated to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment OFF and ON, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient the receiving antenna
Relocate the computer with respect to the receiver
Move the computer away from the receiver
Plug the computer into a different outlet so that the computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to identify and Resolve Radio/TV Interference Problems.

This booklet is available from the U.S. Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class B prescrites dans le Règlement sur le brouillage radioélectrique édicté par le ministère des Communications du Canada.

Lexicon Inc. ● 3 Oak Park ● Bedford, MA 01730-1441 ● Tel (781) 280-0300 ● Customer Service Fax (781) 280-0499
Lexicon Part # 070-15026 Rev 0
Printed in the United States of America

Safety Suggestions

Read Instructions Read all safety and operating instructions before operating the unit.

Retain Instructions Keep the safety and operating instructions for future reference.

Heed Warnings Adhere to all warnings on the unit and in the operating instructions.

Follow Instructions Follow operating and use instructions.

Heat Keep the unit away from heat sources such as radiators, heat registers, stoves, etc., including amplifiers which produce heat.

Ventilation Make sure that the location or position of the unit does not interfere with its proper ventilation. For example, the unit should not be situated on a bed, sofa, rug, or similar surface that may block the ventilation openings; or, placed in a cabinet which impedes the flow of air through the ventilation openings.

Wall or Ceiling Mounting Do not mount the unit to a wall or ceiling except as recommended by the manufacturer.

Power Sources Connect the unit only to a power supply of the type described in the operating instructions, or as marked on the unit.

Grounding or Polarization* Take precautions not to defeat the grounding or polarization of the unit's power cord.
*Not applicable in Canada.

Power Cord Protection Route power supply cords so that they are not likely to be walked on or pinched by items placed on or against them, paying particular attention to cords at plugs, convenience receptacles, and the point at which they exit from the unit.

Nonuse Periods Unplug the power cord of the unit from the outlet when the unit is to be left unused for a long period of time.

Water and Moisture Do not use the unit near water — for example, near a sink, in a wet basement, near a swimming pool, near an open window, etc.

Object and liquid entry Do not allow objects to fall or liquids to be spilled into the enclosure through openings.

Cleaning The unit should be cleaned only as recommended by the manufacturer.

Servicing Do not attempt any service beyond that described in the operating instructions. Refer all other service needs to qualified service personnel.

Damage requiring service The unit should be serviced by qualified service personnel when: the power supply cord or the plug has been damaged, objects have fallen, or liquid has been spilled into the unit, the unit has been exposed to rain, the unit does not appear to operate normally or exhibits a marked change in performance, the unit has been dropped, or the enclosure damaged.

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in these instructions violates safety standards of design manufacture and intended use of the instrument. Lexicon assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT

To minimize shock hazard the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor AC power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

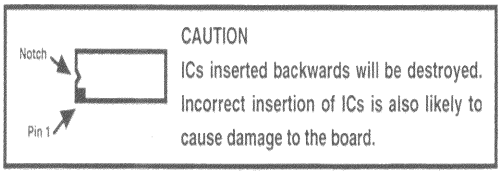
Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing and adjusting.



SAFETY SYMBOLS

General definitions of safety symbols used on equipment or in manuals.

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage. (Terminals fed from the interior by voltage exceeding 1000 volts must be so marked.)

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE:

The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like which is essential to highlight.

CAUTION

Electrostatic Discharge (ESD) Precautions

The following practices minimize possible damage to ICs resulting from electrostatic discharge or improper insertion.

- Keep parts in original containers until ready for use.
- Avoid having plastic, vinyl or styrofoam in the work area.
- Wear an anti—static wrist-strap.
- Discharge personal static before handling devices.
- Remove and insert boards with care.
- When removing boards, handle only by non-conductive surfaces and never touch open-edge connectors except at a static-free workstation.*
- Minimize handling of ICs.
- Handle each IC by its body.
- Do not slide ICs or boards over any surface.
- Insert ICs with the proper orientation, and watch for bent pins on ICs.
- Use static shielding containers for handling and transport.

'To make a plastic-laminated workbench anti-static, wash with a solution of Lux liquid detergent, and allow drying without rinsing.

Table of Contents

Chapter 1 Reference Documents, Required Equipment

Reference Documents

MPX 110 Owner's Manual - Lexicon P/N 070-14956, latest revision

Required Equipment

TOOLS

The following is a minimum suggested technician's tool kit required for performing disassembly, assembly and repairs:

- Clean, antistatic, well lit work area.
- #1 Phillips tips screwdriver
- 3/16” Hex Nut Driver,
- TORX T9 screwdriver
- Hex Nut Driver with 15mm socket.
- 5/16” Hex Nut driver, full hollow
- Plastic insert for the 5/16” nut driver to prevent Front Panel from scratches.
- Solder: 63/37 - Tin/Lead Alloy composition, low residue, no-clean solder.
- Magnification glasses and lamps
- SMT Soldering / Desoldering bench-top repair station

TEST EQUIPMENT

The following is a *minimum* suggested equipment list required to perform the proof of performance tests.

- Digital Volt Meter
- Low Distortion Sine Wave Audio Oscillator
- Distortion Analyzer and Level Meter with single-ended or balanced input, switchable 30kHz high-pass filer or audio bandpass (20-20kHz) filter
- Stereo Headphone Amplifier
- 2 Audio cables unbalanced and shielded with phone plugs on one end and appropriate connectors on the opposite ends for headphone amplifier input
- 2 Audio cables unbalanced and shielded with phone plugs on one end and appropriate connectors on the opposite ends for the Audio Oscillator output
- 9V AC adapter (Lexicon type or equivalent; 1.9 amp)
- Lexicon Double Footswitch (Lexicon P/N 750-09277) w/15' ¼" phone plug cable configured for tip, ring & sleeve or equivalent.
- Cable (6ft minimum) with 1/4" to 1/4 stereo phone plugs (Switchcraft # 10BK10 or equivalent)

Chapter 2 General Information

Periodic Maintenance

Under normal conditions the *MPX 110* system requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and mild detergent to clean the exterior surfaces of the connector box.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners. Avoid using abrasive materials such as steel wool or metal polish. It the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the unit's exterior.

Ordering Parts

When ordering parts, identify each part by type, price and Lexicon Part Number. Replacement parts can be ordered from:

LEXICON, INC.
3 Oak Park
Bedford, MA 01730-1441
Telephone: 781-280-0300; Fax: 781-280-0499; email: csupport@lexicon.com
ATTN: Customer Service

Returning Units to Lexicon for Service

Before returning a unit for warranty or non-warranty service, consult with Lexicon Customer Service to determine the extent of the problem and to obtain Return Authorization. No equipment will be accepted without Return Authorization from Lexicon.

If Lexicon recommends that an *MPX 110* be returned for repair and you choose to return the unit to Lexicon for service, Lexicon assumes no responsibility for the unit in shipment from the customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured and consigned, prepaid, to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company Name
- Street Address
- City, State, Zip Code, Country
- Telephone number (including area code and country code where applicable)
- Serial Number of the unit
- Description of the problem
- Preferred method of return shipment
- Return Authorization #, on both the inside and outside of the package

Please enclose a brief note describing any conversations with Lexicon personnel (indicate the name of the person at Lexicon) and give the name and telephone daytime number of the person directly responsible for maintaining the unit.

Do no include accessories such as manuals, audio cables, footswitches, etc. with the unit, unless specifically requested to do so by Lexicon Customer Service personnel.

Chapter 3 Specifications

Analog Inputs (2)

Connectors: 1/4" unbalanced
Impedance: 500K unbalanced for Direct Instrument input (unit detects a mono input on the right input)
A/D Dynamic Range: >95dB typical, 20Hz-20kHz, unweighted
Levels: -30dBu to +4dBu
Resolution: 24-Bit

Analog Outputs (2)

Connectors: 1/4" unbalanced
Impedance: 75 Ohms for Headphone output (Right only used for mono output; Left only used for stereo headphones)
D/A Dynamic Range: >100dB typical, 20Hz-20kHz, unweighted
Levels : +8dBu typical
Resolution: 24-Bit

Frequency Response: Wet/Dry 20Hz-20kHz, ±1dB
Crosstalk: >45dB
THD: <0.05%, 20Hz-20kHz

Digital Audio Interface

Output Connectors: Coaxial, RCA type; 24-bit Digital S/PDIF (always active)
Sample Rates: 44.1kHz

Internal Audio Data Path: DSP: 24-bit

Footswitch: Tip/Ring/Sleeve phone jack for Bypass and Tap (optional)

System Specifications

Power Requirements: 9VAC wall transformer provided in North America and Europe
No-transformer option available
Environment
Operating Temperature: 32° to 104° (0° to 40°C)
Relative Humidity: 95% non-condensing
Dimensions: 19"W x 1.75"H x 4" D (483x45x102mm)
Weight: Unit: 2lbs, 2 ounces (0.959kg)

Chapter 4 Performance Verification

This section describes procedures to verify the operation of the MPX 110 and the integrity of its analog and digital audio signal paths.

Functional Tests

INITIAL INSPECTION

Inspect the unit for any obvious signs of physical damage. Verify that the front panel controls operate smoothly and correctly. (Refer to the MPX 110 Owner's Manual for detailed explanations of functionality.) Verify that all screws and rear panel jacks are secure, and inspect the AC power supply for any signs of physical damage.

POWER SUPPLY

1. Remove cover as described in disassembly/reassembly section.
2. Plug the adapter into the MPX 110 and apply power.
3. Set the DMM to measure VD and check the regulated voltages for proper levels.

Supplies	Location	Range
+5 VD	Marked test points to the Right of C6	(4.85-5.25)
+5 VA	Marked test points to the Left of J6	(4.75-5.25)
-5 VA	Marked test points to the Left of J6	(-4.75-5.25)

POWER UP

1. Connect the 9VAC adapter (provided with the MPX 110) between the isolated variable output of the Variac and the MPX 110 rear panel **Power** connector.
2. Verify that AC current draw is <0.1 Amps

On normal power up the MPX 110 will run the following Diagnostic Tests. This Diagnostic Test sequence is displayed on the front panel LEDs for trouble-shooting purposes. If any of the red **Clip** LEDs remain lit, a diagnostic failure has occurred and the MPX 110 should be repaired before proceeding.

Test No.	**Test**	**Edit**	**Bypass**	**Store**	**Tap**
1	ROM Checksum	●	●	●	O
2	SRAM	●	●	O	●
3	Lexichip 3 WCS	●	●	O	O
4	Lexichip 3 Interrupt Timer	●	O	●	●
5	Lexichip 3 Audio Data File	●	O	●	O
8	EEPROM Checksum	O	●	●	●

● =OFF
O =ON

SETUP

1. Connect a 5-pin MIDI cable between the MPX 110 rear panel MIDI IN and OUT/THRU connectors.
2. Connect a dual style 1/4" Footswitch to the MPX 110 rear panel Footswitch jack.
3. Turn the MPX 110 front panel VARIATION knob to **1**2.
4. Press and hold the MPX 110 front panel **Bypass** button while powering on the MPX 110.
5. When the green **Level** LEDs light, release **Bypass**.
6. Verify that the MPX 110 front panel **Edit** and **Bypass** LEDs are lit.

Edit	Bypass	Store	Tap
O	O	●	●

7. Turn VARIATION to **6** and verify that the **Bypass**, and **Store** LEDs are lit.

Edit	Bypass	Store	Tap
●	O	O	●

8. Press **Store** to initiate the Encoder Test.

ENCODER TEST

1. Verify that the green **Level L** LED is lit.
2. Turn the VARIATION encoder clockwise direction one position at a time, and verify that the green **Level L** LED turns off after the encoder has been turned one complete revolution. This indicates successful completion of the VARIATION encoder test. The **Level R** LED should now light.
3. Turn the PROGRAM encoder clockwise one position at a time, and verify that the **Level R** LED turns off after the encoder has been turned one complete revolution. This indicates successful completion of the PROGRAM encoder test.
4. Verify that all of the front panel LEDs are now off.

SWITCH/LED TEST

1. Press and hold down the Right button on the footswitch. Verify that the green **Level R** LED is on. Release the footswitch and verify that the LED turns off.
2. Press and hold down the Left button on the footswitch. Verify that the green **Level L** LED is on. Release the footswitch and verify that the LED turns off.
3. Press and hold the front panel **Bypass** button. Verify that its LED is on. Release **Bypass** and verify that the LED turns off.
4. Press and hold the front panel **Tap** button. Verify that its LED is on. Release **Tap** and verify that the LED turns off.
5. Press and hold the front panel **Store** button. Verify that its LED is on. Release **Store** and verify that the LED turns off. Releasing **Store** also exits the test series and should cause both of the green **Level** LEDs to turn on.

ACD POT TEST

Note: During the ADC Pot Test, each potentiometer must be varied over its entire range from fully counter-clockwise to fully clockwise, and back to fully counter-clockwise within 5 seconds. Otherwise the test will fail due to a time-out error. Be prepared, therefore, to move the **Mix** pot as soon as the test is initiated.

1. In preparation for the test, turn the **Mi**x, **Effects Lvl/Bal** and **Adjust** pots fully counter-clockwise.
2. Turn VARIATION to **7** and verify that the **Bypas**s, **Store** and **Tap** LEDs are on, as shown below.

Edit	Bypass	Store	Tap
●	O	O	O

3. Press **Store** to initiate the ADC Pot Test. The **Level L** LED will light to indicate the test has begun and the **Mix** pot is under test.
4. Move **Mix** from its fully counterclockwise position to fully clockwise, and back within 5 seconds. The **Level L** LED will flash to indicate the **Mix** pot has passed and the **Level R** LED will light.
5. Move **Effect Lvl/Bal** from its fully counterclockwise position to fully clockwise, and back within 5 seconds. The **Level R** LED will flash to indicate the **Effect Lvl/Bal** pot has passed, then both **Level** LEDs will light.
6. Move **Adjust** from its fully counterclockwise position to fully clockwise, and back within 5 seconds. Both **Level** LEDs will flash to indicate the **Adjust** pot has passed, then the **Level** LEDs will light steadily to indicate the ADC Pot Test is complete.

MIDI WRAPAROUND TEST

1. Turn VARIATION to the **9** and verify that the **Edit** and **Tap** LEDs are lit as shown below.

Edit	Bypass	Store	Tap
O	●	●	O

2. Press **Store** to execute the test.
3. The **Level** LEDs will light to indicate the test has been successfully completed.

LISTENING TEST

This test involves running audio through the MPX 110 with and without effects processing. This is helpful in differentiating audio problems in the analog from the digital circuitry. The first part of this test is performed without effects.

1. Connect two audio cables between connect the MPX 110 rear panel Left and Right Outputs and the headphone amplifier Left and Right Inputs.
2. Attach the single end of a Y-connector into the output of the sine wave audio oscillator, and the Y end into the MPX 110 Left and Right Inputs.
3. Set the headphone amplifier volume control to its lowest level.
4. Press and hold down the front panel **Bypass** button while powering on the MPX 110. Continue to hold **Bypass** until the Power On Diagnostics are completed and the green **Level** LEDs light.
5. Turn VARIATION to **1**3, and verify that the **Edi**t, **Bypass** and **Tap** LEDs are on, as shown below.

Edit	Bypass	Store	Tap
O	O	●	O

6. Press Store to execute the test.
7. Input a 1kHz sine wave at 0dBu to the MPX 110.
8. Turn the MPX 110 **Input**, **Mix**, **Output**, **Effect Lvl/Ba**l, and **Adjust** knobs fully clockwise.
9. Put on headphones, then set the headphone amplifier volume to a comfortable listening level.
10. Individually adjust the MPX 110 **Input** and **Output** knobs over their entire range and verify that no pops, clicks, or scratchiness is heard.

EFFECTS LISTENING TEST

1. Turn VARIATION to **14** and press Store to return to normal operating mode.
2. Verify that the processed audio has no audible pops, clicks, or distortion.

SHOCK TEST

1. Lift each corner of the MPX 110 off the bench 4 inches (4") then drop. **To prevent damaging the unit, keep one corner of the unit touching the bench at all times.**
2. Verify that no audio, or LED intermittence is caused by this action.

Audio Performance:

SETUP

Oscillator and Analyzer Default Settings

Unless otherwise noted the following settings are used for the audio performance tests:

Oscillator	**Analyzer**
Waveform: Sine	Filter: Off
Output: Unbal	Bandwidth: 22Hz to 22kHz
–25Ω	Inputs: 100κΩ
Float	(except Gain=600W)

1. Connect the appropriate cable between the oscillator output and the MXP 100 Left input.
2. Connect the appropriate cable between the analyzer input and the MPX 110 Left output.
3. Turn the MPX 110 front panel **Input** and **Output** knobs fully clockwise.
4. Turn the MPX 110 front panel **Mix** knob fully counterclockwise.
5. Power cycle the MPX 110 while pressing and holding down the **Bypass** button. Wait until the **Level** LEDs light, then release **Bypass**.

6. Turn VARIATION to **13** and press **Store** to set up the MPX 110 for the following tests.

GAIN TEST

This test verifies the input-to-output gain characteristic of the MPX 110 through the signal path.

1. Apply a 1kHz signal at 775mV to the MPX 110.
2. Verify 1.95 V +/- 0.05V at the MPX 110 Left output.
3. Connect the oscillator output to the MPX 110 Right input.
4. Connect the analyzer input to the MPX 110 Right output.
5. Verify an output of 1.95V +/- 0.05V at the MPX 110 Right output.

SIGNAL-TO-NOISE TEST

This test checks the signal-to-noise through the MPX 110 signal path.

1. Set the scale on the distortion analyzer to measure -50dBu signal.
2. Disconnect the oscillator from the MPX 110 input, or turn the oscillator off.
3. Verify that the noise floor is <90dBr.
4. Connect the oscillator output to the MPX 110 Left input.
5. Connect the analyzer input to the MPX 110 Left output.
6. Repeat the test, verifying the levels at the Left output.

THD+N

This test verifies THD+N through the MPX 110 signal path.

1. Apply a 1kHz signal at 220mV to the MPX 110 left input.
2. Adjust the scale on the distortion analyzer to measure % THD+N.
3. Verify a distortion level <0.05% THD+N at the Left output.
4. Connect the oscillator output to the MPX 110 right input.
5. Connect the analyzer input to the MPX 110 right output.
6. Verify a distortion level <0.05% THD+N at the right output.

FREQUENCY RESPONSE TEST

This test verifies the frequency response of the MPX 110 through the signal path at 20Hz, 3kHz, 5kHz, and 20kHz.

1. Apply a 220mV signal at 1kHz with the analyzer Bandwidth filters off to the MPX 110 Right input.
2. Use the output level at the MPX 110 Right output for the 0DB reference to check frequency response.
3. Verify that the signal level output is within ±0.5dB of the reference at the above frequencies.
4. Connect the oscillator output to the MPX 110 Left input.
5. Connect the analyzer input to the MPX 110 Left output.
6. Repeat the test, verifying levels for the MPX 110 Left output.

LEXICON AUDIO PRECISION ATE SUMMARY

This chart represents a summary of test Audio Precision test settings and parameters used by Lexicon Manufacturing in production testing of all MPX 200 product. This is provided as a reference and supplement to bench test settings found in the proof of performance in this manual.

A-D Files **Source** **Analyzer**

	Left	Right			Bal /	Gnd /								Sample
Test	**Input**	**Input**	**Freq**	**Imp.**	**Unbal**	**Float**	**Level**	**Reading**	**Upper**	**Lower**	**Filter**	**Imp**	**Band**	**Rate**
a-dgain	-21dBu	-21dBu	997	25 Ohm	Unbal	Float	LEVEL(dBFS)	-1.70	-0.64	-2.54	Off	------	--------	44.1kHz
a-dfreq	-31dBu	-31dBu	20-20k	25 Ohm	Unbal	Float	LEVEL(dBFS)	0	1.06	-1.06	Off	------	--------	44.1Khz
adsetlvl	-20dBu	-20dBu	997	25 Ohm	Unbal	Float	LEVEL(dBFS)	--------	-20.00	-20.50	Off	------	--------	44.1kHz
a-dxtalk*	-11dBu	-11dBu	20-20k	25 Ohm	Unbal	Float	LEVEL(dBFS)	--------	-44.94	-120.0	Off	------	--------	44.1kHz
a-dthd*	-11dBu	-11dBu	20-20k	25 Ohm	Unbal	Float	FLTLVL(%)	--------	0.05	0.0007	Band Rej	------	--------	44.1kHz
a-ddynr*	-50dBu	-50dBu	997	25 Ohm	Unbal	Float	FLTLVL(dBFS)	--------	-89.94	-120.00	Off	------	--------	44.1kHz

A-A Files **Source**
Analyzer

	Left	Right			Bal /	Gnd /								Sample
Test	**Input**	**Input**	**Freq**	**Imp.**	**Unbal**	**Float**	**Level**	**Reading**	**Upper**	**Lower**	**Filter**	**Imp**	**Band**	**Rate**
a-again*	0dBu	0dBu	997	25 Ohm	Unbal	Float	AMPL(dBu)	8.00	9.56	6.44	Off	100k	10-500k	44.1kHz
a-afreql*	-11dBu	-11dBu	20-20K	25 Ohm	Unbal	Float	AMPL(dBr)	0.00	1.06	-1.06	Off	100k	10-500k	44.1kHz
a-afreqr*	-11dBu	-11dBu	20-20K	25 Ohm	Unbal	Float	AMPL(dBr)	0.00	1.06	-1.06	Off	100k	10-500k	44.1kHz
a-axtalk*	-11dBu	-11dBu	20-20K	25 Ohm	Unbal	Float	XTALK(dB)	------	-45	-120	Off	100k	20-22k	44.1kHz
a-athd*	-11dBu	-11dBu	20-20K	25 Ohm	Unbal	Float	THD+N(%)	------	0.05	0.0007	Off	100k	20-22k	44.1kHz
a-asnrl*	0dBu	0dBu	997	25 Ohm	Unbal	Float	AMPL(dBr)	------	-90	-120	Off	100k	20-22k	44.1kHz
a-adynrl*	-50dBu	-50dBu	997	25 Ohm	Unbal	Float	THD+N(dBr)	------	-90	-120	Off	100k	20-22k	44.1kHz
a-asnrr*	0dBu	0dBu	997	25 Ohm	Unbal	Float	AMPL(dBr)	------	-90	-120	Off	100k	20-22k	44.1kHz
a-adynrr*	-50dBu	-50dBu	997	25 Ohm	Unbal	Float	THD+N(dBr)	------	-90	-120	Off	100k	20-22k	44.1kHz
a-amute*	0dBu	0dBu	997	25 Ohm	Unbal	Float	AMPL(dBu)	-38.00	-30.00	-90.00	Off	100k	10-500k	44.1kHz

* The MPX 100 is set for analog to digital unity gain with ADSETLVL test.

Note: For analog testing only, the MPX 110 can be set for analog to analog unity gain using the AASETLVL test.

aasetlvl	0dBu	0dBu	997	25 Ohm	Unbal	Float	AMPL(dBu)	8.00	9.56	6.44	Off	100k	10-500k	44.1kHz

Chapter 5 Troubleshooting

Check the Lexicon web site for the latest software and information:
http://www.lexicon.com

The Lexicon Support Knowledgebase:
http://www.lexicon.com/kbase/index.asp

Diagnostics

INTRODUCTION

This document contains the complete diagnostics descriptions for the Lexicon MPX 110 product.

DIAGNOSTICS TEST DESCRIPTIONS

There are two categories of diagnostics that exist in the MPX 110 software: (1) Power On (automatic) Diagnostics and (2) Functional Tests/Extended Diagnostics. As you might expect, the Power Up Diagnostics will be executed automatically everytime the system is powered on. The Functional Tests/Extended Diagnostics will be invoked by pressing and holding down the **BYPASS** button while powering on the unit until the **green level leds** stay on.

POWER ON DIAGNOSTICS

Upon normal power on, all of the Front Panel LED's will be turned on for approximately 200ms, and then the MPX 110 will attempt to run the sequence of diagnostic tests listed in table 1 below. These diagnostic tests have been designed to take less than 10 seconds.

During the execution of the Power On Diagnostics, the CPU (wherever possible) will display a test code on the EDIT, BYPASS, STORE & TAP LED's prior to the execution of the test (provided the LED's are functioning properly).

Throughout this document, Edit, Bypass, Store, and Tap LED's will be referred to as the Binary LED's. These LED's are used to display the binary value of the corresponding test number. This value is sent to the Binary LED's before each test is executed. Displaying the test/error code on the LED's before the test is executed, makes it possible to determine which test failed if the unit hangs or crashes during the test.

Test No.	Test	Edit	Bypass	Store	Tap
1	**ROM Checksum**	O	O	O	●
2	**SRAM**	O	O	●	O
3	**Lexichip3 WCS**	O	O	●	●
4	**Lexichip3 Interrupt Timer**	O	●	O	O
5	**Lexichip3 Audio Data File**	O	●	O	●
6	**EEPROM Checksum**	●	O	O	O

Table 1.

When the Power On Diagnostic tests have completed, the software version will flash on the Front Panel Binary LED's for approximately two seconds.

Note: The Binary LED's are interrupt driven. Therefore, the ROM, SRAM, LEXICHIP 3 & CPU must be working properly in order for the Binary LED's to operate correctly.

DIAGNOSTIC FAILURES

When a failure is encountered during the test sequence:

- The test code is displayed on the Binary LED's (Ref. Table 1).

- The Clip (red) Headroom LED's are turned on to indicate a failure has occurred.

- The unit stops executing the Power On Diagnostic test sequence.

- The audio outputs are muted, and the unit will not become operational.

If the **BYPASS** button is pressed after a failure has occurred, the MPX 110 will attempt to continue on with the next test of the Power On Diagnostic test sequence, and the MPX 110 will attempt to do this every time the **BYPASS** button is pressed.

If the **STORE** button is pressed after a failure has occurred, the MPX 110 will enter the Extended Diagnostics mode.

If the **TAP** button is pressed after a failure has occurred, the MPX 110 will run the test continuously.

The following diagram describes the Binary LED's:

Edit	**Bypass**	**Store**	**Tap**
O	O	●	●
MSB			**LSB**

LED Off = O (0)
LED On = ● (1)

Figure 1.

This figure shows an example of the Binary LED's Failure Code 3 (0011). This code indicates that the Lexichip3 WCS Test has failed.

ROM CHECKSUM TEST (1)

The ROM checksum, is a byte size value that is stored in the last location of Bank 0. The test adds the contents of the entire ROM including the Checksum byte. The result should equal zero (8 bit value).

Before the test is executed, a test code will be put out on the Binary LED's. The code is:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

If a failure occurs, the Clip (red) headroom LED's will be turned on in addition to the binary code, and the CPU will attempt to continuously loop the test for troubleshooting purposes.

If the **BYPASS** button is pressed, the failure is ignored and the next test will be executed.

SRAM TEST (2)

The SRAM Test performed during the Power On Diagnostics is a destructive test. The entire contents of the SRAM is tested by first writing 00 hex (00000000 binary) to all of the memory locations, and then verified by reading back all of the memory locations. This write/read sequence is also performed using the following

patterns: 55 hex (01010101 binary), AA hex (10101010 binary) & FF hex (11111111 binary).

Before the test is executed, a test code will be put out on the Binary LED's. The code is:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

If a failure occurs, the Clip (red) headroom LED's will be turned on in addition to the binary code, and the CPU will attempt to continuously loop the test for troubleshooting purposes.

If the **BYPASS** button is pressed, the failure is ignored and the next test will be executed.

LEXICHIP3 WCS TEST (3)

This test will check the RAM program memory space (writeable control store) of the Lexichip3. The WCS (memory space) is first filled with the value 55 hex (01010101 binary), then each memory location is read to see if it contains 55. If 55 is in the memory location, the location is filled with AA hex (10101010 binary), and the next location is processed. Once the RAM has been checked for 55's and filled with AA's, the process is then repeated checking for AA's and storing 0's into memory. Following this test an Address test is performed to verify all the address lines are active. Finally, the memory is checked for 0's.

Before the test is executed, a test code will be displayed on the Binary LED's. The code is:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

If a failure occurs, the Clip (red) headroom LED's will be turned on in addition to the binary code.

If the **BYPASS** button is pressed, the failure is ignored and the next test will be executed.

If the **TAP** button is pressed, the CPU will attempt to go into a mode where it can execute the test continuously.

LEXICHIP3 INTERRUPT TIMER TEST (4)

The Interrupt Timer test will verify that the interrupt (INT/) is working and occurring at the proper intervals. The Lexichip3 will provide the MPX 110 with the interrupt (INT/) to the Z80's maskable interrupt line. The interrupt test will be run for a period of time that allows 20 interrupts to occur. A count of the interrupts is kept and compared for overshoot and undershoot. Greater than 21 interrupts means the interrupt is too short and less than 19 interrupts means it's too long.

Before the test is executed, a test code will be put out on the Binary LED's. The code is:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

If a failure occurs, the Clip (red) headroom LED's will be turned on in addition to the binary code.

If the **BYPASS** button is pressed, the failure is ignored and the next test will be executed.

If the **TAP** button is pressed, the CPU will attempt to go into a mode where it can execute the test continuously.

LEXICHIP3 AUDIO DATA FILE TEST (5)

The Audio Data File (ADF) is a fast synchronous 128-word SRAM that provides audio data buffering and storage for: external memory references, Serial I/O, and the Host-to-Lexichip data port. ADF locations also function as ARU Registers and as scratchpad memory. This test will verify that the Lexichip3 Audio Data File is working properly.

Before the test is executed, a test code will be put out on the Binary LED's. The code is:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

If a failure occurs, the Clip (red) headroom LED's will be turned on in addition to the binary code.

If the **BYPASS** button is pressed, the failure is ignored and the next test will be executed.

If the **TAP** button is pressed, the CPU will attempt to go into a mode where it can execute the test continuously.

EEPROM CHECKSUM (8)

This test will read each byte in the User Register portion of the EEPROM and add them together to calculate a checksum. This value is compared with the checksum value stored in the EEPROM itself. This checksum will be recalculated each time a register is stored.

The test will also verify that the EEPROM has been initialized properly. This is done by storing the software version of the EPROM in the first five bytes of the EEPROM, and then verifying the stored value is correct when the test is executed. If the stored value read from the first five bytes of the EEPROM is incorrect, the EEPROM will be initialized.

Before the test is executed, a test code will be put out on the Binary LED's. The code is:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

If a failure occurs, the Clip (red) headroom LED's will be turned on in addition to the binary code.

If the **BYPASS** button is pressed, the failure is ignored and the next test will be executed.

If the **TAP** button is pressed, the CPU will attempt to go into a mode where it can execute the test continuously.

EXTENDED DIAGNOSTICS

The following tests are available in the Extended Diagnostics:

Test Number	Test Name	Binary LED's	See Note:
1	**ROM Checksum**	0 0 0 1	1
2	**SRAM Test**	0 0 1 0	1
3	**Lexichip3 WCS**	0 0 1 1	1
4	**Lexichip3 Interrupt Timer**	0 1 0 0	1
5	**Lexichip3 Audio Data File**	0 1 0 1	1
6	**Encoder/Switch/LED**	0 1 1 0	2
7	**ADC Pot**	0 1 1 1	3
8	**EEPROM**	1 0 0 0	
9	**MIDI**	1 0 0 1	
10	**LED** (for troubleshooting)	1 0 1 0	2
11	**Lexichip3 External DRAM**	1 0 1 1	
12	**Burn In Loop**	1 1 0 0	
13	**Audio I/O**	1 1 0 1	
14	**Exit Diagnostics**	1 1 1 0	
15	**Initialize**	1 1 1 1	

NOTES:

1. These tests reside in the Power On Diagnostics.

2. These tests require operator interaction and judgment. Doesn't generate any error messages.

3. This test requires operator interaction and judgment. Generates an error message.

The Extended Diagnostics will be invoked by pressing & holding the **BYPASS** button while powering on the unit. When the L & R Level (green) LED's are lit, release the **BYPASS** button. After the **BYPASS** button is released, the Binary LED's (EDIT, BYPASS, STORE & TAP) will display the current position of the **VARIATION** knob in binary and the Level (green) LED's will go off.

For example, if the **VARIATION** knob was set to 5, the LED's would read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

When a test is selected, the **STORE** button must be pressed to execute it. If the test passed, the L & R Level (green) LED's will light. If the test failed, the L & R Clip (red) LED's will light.

The following tests can be run continuously by pressing the **TAP** button instead of the **STORE** button.

Test Number	Test Name	Binary LED's
1	**ROM Checksum**	**0 0 0 1**
2	**SRAM Test**	**0 0 1 0**
3	**Lexichip3 WCS**	**0 0 1 1**
4	**Lexichip3 Interrupt Timer**	**0 1 0 0**
5	**Lexichip3 Audio Data File**	**0 1 0 1**
8	**EEPROM**	**1 0 0 0**
9	**MIDI**	**1 0 0 1**
11	**Lexichip3 External DRAM**	**1 0 1 1**

When a test is run continuously a pass/fail status will be displayed and updated on the headroom LED's each time the test is run. If the test passed, the L & R Level (green) LED's will light. If the test failed, the L & R Clip (red) LED's will light.

To stop the test from running continuously, press the **STORE** button.

ROM CHECKSUM TEST (1)

This is the same test that resides in the power up diagnostics. It was included in the Extended Diagnostics for troubleshooting purposes.

The ROM checksum, which is a byte size value, will be located as the last location of Bank 0. The test will add the contents of the entire ROM including the Checksum byte. The result should equal zero (8 bit value).

When selected, the Binary LED's will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

Pressing the **TAP** button will run the test continuously

The remaining buttons, encoders, ADC Pots and footswitches (2) are inactive. When the test is executed, all Front Panel LED's will go off.

If the test passed, the L & R Level (green) LED's will light.

If the test failed, the Left Clip (red) LED will light.

To run the test again, press the **STORE** button.

To run the test continuously, press the **TAP** button.

To stop the test from running continuously, press the **STORE** button.

SRAM TEST (2)

The SRAM Test performed during the Extended Diagnostics is a non-destructive test. The non-destructive test will test one memory location at a time, saving the contents from the location being tested into a register, and then restoring the value when it's done. The entire contents of the SRAM is tested by writing 00 hex (00000000 binary), and verified by reading the same value back from each memory location. This write/read sequence is also performed using the following patterns: 55 hex (01010101 binary), AA hex (10101010 binary) & FF hex (11111111 binary).

This test was included in the Extended Diagnostics for troubleshooting purposes.

When selected, the Binary LED's will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

Pressing the **TAP** button will run the test continuously

The remaining buttons, encoders, ADC Pots and footswitches (2) are inactive. When the test is executed, all Front Panel LED's will go off.

If the test passed, the L & R Level (green) LED's will light.

If the test failed, the L & R Clip (red) LED's will light.

To run the test again, press the **STORE** button.

To run the test continuously, press the **TAP** button.

To stop the test from running continuously, press the **STORE** button.

LEXICHIP3 WCS TEST (3)

This is the same test that resides in the power on diagnostics. It was included in the Extended Diagnostics for troubleshooting purposes.

This test will check the RAM program memory space (writeable control store) of the Lexichip3. The WCS (memory space) is first filled with the value 55 hex (01010101 binary), then each memory location is read to see if it contains 55. If 55 is in the memory location, the location is filled with AA hex (10101010 binary), and the next location is processed. Once the RAM has been checked for 55's and filled with AA's, the process is then repeated checking for AA's and storing 0's into memory. Following this test is an Address test to verify all the address lines are active. Finally, the memory is checked for 0's.

When selected, the Binary LED's will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

Pressing the **TAP** button will run the test continuously

The remaining buttons, encoders, ADC Pots and footswitches (2) are inactive. When the test is executed, all Front Panel LED's will go off.

If the test passed, the L & R Level (green) LED's will light.

If the test failed, the L & R Clip (red) LED's will light.

To run the test again, press the **STORE** button.

To run the test continuously, press the **TAP** button.

To stop the test from running continuously, press the **STORE** button.

LEXICHIP3 INTERRUPT TIMER TEST (4)

This is the same test that resides in the power on diagnostics. It was included in the Extended Diagnostics for troubleshooting purposes.

The Interrupt test will verify that the interrupt (ZINT/) is working and occurring at the proper intervals. The Lexichip3 will provide MPX 110 with the interrupt (ZINT/) to the Z80's maskable interrupt line. The interrupt test will run for a period of time that allows 20 interrupts to occur. A count of the interrupts is kept and compared for overshoot and undershoot. Greater than 21 interrupts means the interrupt is too short and less than 19 interrupts means it's too long.

When selected, the Binary LED's will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

Pressing the **TAP** button will run the test continuously

The remaining buttons, encoders, ADC Pots and footswitches (2) are inactive. When the test is executed, all Front Panel LED's will go off.

If the test passed, the L & R Level (green) LED's will light.

If the test failed, the L & R Clip (red) LED's will light.

To run the test again, press the **STORE** button.

To run the test continuously, press the **TAP** button.

To stop the test from running continuously, press the **STORE** button.

LEXICHIP3 AUDIO DATA FILE TEST (5)

This is the same test that resides in the power on diagnostics. It was included in the Extended Diagnostics for troubleshooting purposes.

This test will verify that the Lexichip3 Audio Data File memory is working.

The Audio Data File (ADF) is a fast synchronous 128-word SRAM that provides audio data buffering and storage for: external memory references, Serial I/O, and the Host-to-Lexichip data port. ADF locations also function as ARU Registers and as scratchpad memory. This test will verify that the Lexichip3 Audio Data

File is working properly.

When selected, the Binary LED's will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **TAP** button will run the test continuously

The remaining buttons, encoders, ADC Pots and footswitches (2) are inactive. When the test is executed, all Front Panel LED's will go off.

If the test passed, the L & R Level (green) LED's will light.

If the test failed, the L & R Clip (red) LED's will light.

To run the test again, press the **STORE** button.

To run the test continuously, press the **TAP** button.

To stop the test from running continuously, press the **STORE** button.

ENCODER/SWITCH/LED TEST (6)

The Encoder/Switch/LED Test is essentially three tests in one. The combination of the three tests provides a means for verifying the operation of the Encoders (2), Front Panel Buttons (3) and Footswitches (2) at the same time. Refer to table 3 for Encoder Gary scale when debugging.

When selected, the display will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

When the test is executed, the Left Level (green) LED will be lit, and all Front Panel LED's will be turned off.

IMPORTANT: The Encoder/Switch/LED Test MUST be performed in the proper sequence. The Encoder portion of the test MUST be performed first, before any Switch or LED testing can be performed.

Encoders:

When the test is executed the CPU reads the value of the encoder being tested, and then expects the next value read from the encoder (when the encoder position is changed) will be at a predetermined incremental value. Therefore, during the test each encoder must be rotated in a clockwise direction as it's being tested, or the test will fail.

When the Encoder Test is first executed, the Left Level (green) LED will be lit to indicate that the **VARIATION** Encoder is being tested.

When the **VARIATION** Encoder has been rotated clockwise over its entire range, the Left Level (green) LED will be turned off to indicate the **VARIATION** Encoder has passed, and the Right Level (green) LED will be turned on.

If the **VARIATION** Encoder fails, the Left Clip (red) LED will light.

Once the **VARIATION** Encoder has passed, the Right Level (green) LED will be lit to indicate that the **PROGRAM** Encoder is being tested.

When the **PROGRAM** Encoder has been rotated clockwise over its entire range, the Right Level (green) LED will be turned off to indicate that the **PROGRAM** Encoder has passed, and the Front Panel Switches and Footswitches are ready to be tested.

If the **PROGRAM** Encoder fails, the Right Clip (red) LED will light.

Note: During the Encoder Test, the Front Panel Binary LED's will display the current position of the Encoder under test in binary. (See Table 2)

PROGRAM Encoder Position	VARIATION Encoder Position	Binary LED's
Plate, Gate	1	0 0 0 1
Hall, Chamber	2	0 0 1 0
Ambience, Room	3	0 0 1 1
Tremelo, Rotary	4	0 1 0 0
Chorus, Flange	5	0 1 0 1
Pitch, Detune	6	0 1 1 0
Delay, Echo	7	0 1 1 1
Special FX	8	1 0 0 0
User	9	1 0 0 1
Flange - Delay	10	1 0 1 0
Pitch - Delay	11	1 0 1 1
Chorus - Delay	12	1 1 0 0
Delay - Reverb	13	1 1 0 1
Flange - Reverb	14	1 1 1 0
Pitch - Reverb	15	1 1 1 1
Chorus - Reverb	16	0 0 0 0

Table 2.

Footswitches:

When the left footswitch (labeled Ring) is pressed, the left Level (green) LED will light. The remaining LED's will be off. When the left footswitch is released, the left Level (green) LED will go off and the remaining LED's will be off as well.

When the right footswitch (labeled Tip) is pressed, the right Level (green) LED will light. The remaining LED's will be off. When the right footswitch is released, the right Level (green) LED will go off and the remaining LED's will be off as well.

To exit the test, press the **STORE** button. The binary LED's will then display the current position of the **VARIATION** Encoder.

Front Panel Switches:

When the **BYPASS** button gets pressed, its LED will light and the remaining LED's will go off. When the **BYPASS** button is released, its LED will go off and the remaining LED's will be off as well.

When the **TAP** button gets pressed, its LED will light and the remaining LED's will be off. When the **TAP** button is released, its LED will go off and the remaining LED's will be off as well.

When the **STORE** button gets pressed, its LED will light and the remaining LED's will be off. When the **STORE** button is released, its LED will go off and the test will be exited.

Encoder Gray Scale

The following table is provided as a reference for debugging encoder problems.

Encoder Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin 1	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**
Pin 2	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
Pin 3	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**
Pin 4	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Pin 5	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Table 3.

Note: The logic levels from the encoders are only valid when the enable (pin 5) is low.

ADC POT TEST (7)

The **MIX**, **EFFECTS LVL/BAL** and **ADJUST** Pots are connected to integrating type ADC's (A/D Converters) and are read digitally by the Lexichip3. The ADC Pot Test will verify that the pots and converters are working.

While performing the ADC Pot Test, the ADC Pot under test must be varied over its entire range from fully counter-clockwise to fully clockwise and back to fully counter-clockwise (CCW-CW-CCW).

During the rotation of the ADC Pot under test, the data generated by the ADC circuitry during the sweep will be analyzed and confirm that the circuit is accurately reporting the data to the Lexichip3. When the (CCW-CW-CCW) sweep has been completed successfully, the test will display a Pass, Fail or Timeout status on the headroom (L & R Level & Clip (red) LED's).

When an ADC Pot is being tested, the ADC Pot must be swept over its entire (CCW-CW-CCW) range within five seconds. Otherwise, after 5 seconds the headroom LED's will indicate that a Timeout Failure has occurred.

When selected, the Front Panel LED's will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

When the test is executed the remaining buttons, encoders, ADC Pots and footswitches (2) are inactive, and all Front Panel LED's will go off.

The **STORE** button will be active to exit the test.

MIX Pot Pass/Fail Status:

The Left Level (green) LED will be lit to indicate when the **MIX** Pot is being tested. The remaining LED's will be off.

If the **MIX** Pot passes the test, the Left Level (green) LED will flash about 2 times per second.

If the **MIX** Pot fails the test, the Left Clip (red) LED will flash about 2 times per second.

If the **MIX** Pot exhibits a timeout failure, the Left Level & Clip (red) LED's will flash about 2 times per second.

EFFECTS LVL/BAL Pot Pass/Fail Status:

The Right Level (green) LED will be lit to indicate when the **EFFECTS LVL/BAL** Pot is being tested. The remaining LED's will be off.

If the **EFFECTS LVL/BAL** Pot passes the test, the Right Level (green) LED will flash about 2 times per second.

If the **EFFECTS LVL/BAL** Pot fails the test, the Right Clip (red) LED will flash about 2 times per second.

If the **EFFECTS LVL/BAL** Pot exhibits a timeout failure, the Right Level & Clip (red) LED's will flash about 2 times per second.

ADJUST Pot Pass/Fail Status:

The L & R Level (green) LED's will be lit to indicate when the **ADJUST** Pot is being tested. The remaining LED's will be off.

If the **ADJUST** Pot passes the test, the L & R Level (green) LED's will flash about 2 times per second.

If the **ADJUST** Pot fails the test, the L & R Clip (red) LED's will flash about 2 times per second.

If the **ADJUST** Pot exhibits a timeout failure, the L & R Level and L & R Clip (red) LED's will flash about 2 times per second.

After the **MIX**, **EFFECTS LVL/BAL** and **ADJUST** pots have all been tested, the headroom LED's will display the pass/fail status of the test.

The L & R Level (green) LED's will be lit to indicate the test has passed, or the L & R Clip (red) LED's will be lit to indicate the test has failed.

EEPROM CHECKSUM (8)

This is the same test that resides in the power on diagnostics. It was included in the Extended Diagnostics for troubleshooting purposes.

This test will read each byte in the User Register portion of the EEPROM and add them together to calculate a checksum. This value is compared with the checksum value stored in the EEPROM itself. This checksum will be recalculated each time a register is stored.

The test will also verify that the EEPROM has been initialized properly. This is done by storing the software version of the EPROM in the first five bytes of the EEPROM, and then verifying the stored value is correct when the test is executed. If the stored value read from the first five bytes of the EEPROM is incorrect, the EEPROM will be initialized.

When selected, the Binary LED's will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

When the test is executed the remaining buttons, encoders, ADC Pots and footswitches (2) are inactive, and all Front Panel LED's will go off.

If the test passed, the L & R Level (green) LED's will light.

If the test failed, the L & R Clip (red) LED's will light.

To run the test again, press the **STORE** button.

To run the test continuously, press the **TAP** button.

To stop the test from running continuously, press the **STORE** button.

MIDI TESTS (9)

MIDI Out To MIDI In

This test will verify that the MIDI Input and MIDI Output/Thru circuits are working. The test will transmit data out of the MIDI OUT jack and will attempt to read the data through the MIDI IN jack. To run this test, a 5 Pin Male DIN to 5 Pin Male DIN Cable (also known as a MIDI cable) must be connected between the MIDI IN jack and the MIDI OUT jack. MIDI Input and MIDI Output/Thru comes from the Lexichip3.

When selected, the Binary LED's will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

When the test is executed the remaining buttons, encoders, ADC Pots and footswitches (2) are inactive, and all Front Panel LED's will go off.

If the test passed, the L & R Level (green) LED's will light.

If the test failed, the L & R Clip (red) LED's will light.

To run the test again, press the **STORE** button.

To run the test continuously, press the **TAP** button.

To stop the test from running continuously, press the **STORE** button.

MIDI Thru To MIDI In

The MIDI Thru circuitry is tested during the ATE testing, a MIDI command is sent to the MPX 110 which sets the MIDI Out/MIDI Thru to MIDI Thru. The default setting for the MIDI Out/MIDI Thru is MIDI Out.

Using the APUTIL.EXE program utility with command arguments from DOS prompt you can test MIDI I/O. APUTIL M allows you to transmit MIDI data from PC. The APUTIL M T command is a self contained test for MIDI THRU and wrap around (for information on APUTIL, refer to document 010-09629). The MIDI OUT cable from the Audio Precision's PC (MPU-401 Card) will be connected to the MIDI IN connector on the MPX 110. The MIDI IN cable from the Audio Precision's PC will be connected to the MIDI OUT/MIDI THRU connector on the MPX 110.

When the APUTIL M T command is executed, the MIDI Output from the PC will produce a message (F8 for example) in which the message will get reproduced at the MPX 110's MIDI THRU jack. The PC will read and verify the message was received from the MPX 110's MIDI THRU jack. The test can be easily be run by entering the command APUTIL M T F8 (or any other byte except for FF) in the Audio Precision's DOS

mode or from the PC's command line.

LED TEST (10)

This test will verify all LED's (8) are working. When selected, the Binary LED's will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

When the test is executed, the Front Panel LED's that are assigned to the current position of the **PROGRAM** Encoder will be lit. (See below)

PROGRAM Encoder Position	LED Assignment
Plate, Gate	**All LED's On**
Hall, Chamber	**Left Clip On**
Ambience, Room	**Right Clip On**
Tremelo, Rotary	**Left Level On**
Chorus, Flange	**Right Level On**
Pitch, Detune	**Edit On**
Delay, Echo	**Bypass On**
Special FX	**Store On**
User	**Tap On**
Flange - Delay	**All LED's Off**
Pitch - Delay	**All LED's Off**
Chorus - Delay	**All LED's Off**
Delay - Reverb	**All LED's Off**
Flange - Reverb	**All LED's Off**
Pitch - Reverb	**All LED's Off**
Chorus - Reverb	**All LED's Off**

The **STORE** button will be active to exit the test. The **PROGRAM** Encoder will be active to test the LED's. Referring to Table 2, each LED is assigned to a position on the **PROGRAM** Encoder. When a position is selected, its assigned LED will light. There's also a position where all the LED's will light and a position where all LED's are off.

When the test is executed the VARIATION Encoder, BYPASS, TAP, ADC Pots and footswitches (2) are inactive.

LEXICHIP3 EXTERNAL DRAM TEST (11)

The DRAM test is a modified checksum test executed by the Lexichip3, and is designed to exercise all 24 of the DRAM data bits. During the test, a unique value is written into each memory location, a modified checksum which alternately adds or subtracts successive values is then calculated and stored in the Lexichip3's ADF. The checksum calculated from all the DRAM memory locations is then compared with the checksum stored in the Lexichip3's ADF. The test passes if the DRAM checksum equals what is stored in the Lexichip3's ADF. The DRAM test takes approximately 12 seconds to complete.

Note: Interrupts are disabled during the test which effect the normal operation of the Front Panel LED's. The Front Panel LED's will return to normal operation when the test is completed and the pass/fail result is displayed.

When selected, the Binary LED's will read the following:

Edit	Bypass	Store	Tap
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

When the test is executed the remaining buttons, encoders, ADC Pots, and footswitches (2) are inactive, and all Front Panel LED's will go off.

If the test passed, the L & R Level (green) LED's will light.

If the test failed, the L & R Clip (red) LED's will light.

To run the test again, press the **STORE** button.

To run the test continuously, press the **TAP** button.

To stop the test from running continuously, press the **STORE** button.

BURN IN LOOP (12)

The Burn In Loop will continuously run the following diagnostics:

Test Number	Test Name	Binary LED's
1	**ROM Checksum**	**0 0 0 1**
2	**SRAM Test**	**0 0 1 0**
3	**Lexichip3 WCS**	**0 0 1 1**
4	**Lexichip3 Interrupt Timer**	**0 1 0 0**
5	**Lexichip3 Audio Data File**	**0 1 0 1**
11	**Lexichip3 External DRAM**	**1 0 1 1**

When selected, the Binary LED's will read the following:

Edit	Bypass	Store	Tap
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

When the test is executed the remaining buttons, encoders, ADC Pots and footswitches (2) are inactive.

During the execution of the Diagnostics in the Burn In loop, the appropriate test code will be displayed on the binary LED's. This code will be sent to the LED's before each test is executed. By displaying a test/error code on the LED's before the test is activated, it will be easier to determine which test failed if the unit hangs or crashes during the Burn In Loop.

If a test failed, the Burn In Loop will stop and the Binary LED's will display which test failed along with the L & R Clip (red) LED's lit.

There are three options available when a test has failed during the Burn In Loop:

1. Press the **BYPASS** button to continue the Burn In Loop.
2. Press the **TAP** button to run the test continuously.
3. Press the **STORE** button to exit the Burn In Loop.

AUDIO I/O (13)

The Audio I/O Test will set the audio path through the MPX 110 for 100% WET signal without any effects. By using this test, the technician can eliminate major functional sections of the system when troubleshooting gain, crosstalk, frequency response, distortion and noise problems in a system.

When selected, the Binary LED's will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

When the test is executed the L & R Level (green) LED's are lit, and the test number is displayed on the Binary LED's. The remaining buttons, encoders, ADC Pots and footswitches (2) are inactive.

Note: The Audio I/O mode sets the MIDI Out/Thru system parameter to MIDI Thru mode.

EXIT DIAGNOSTICS (14)

This selection will allow the user to exit the Extended Diagnostic Mode into normal operating mode. When selected, the Binary LED's will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

When the selection is executed the remaining buttons, encoders, ADC Pots and footswitches (2) are inactive, and the MPX 110 will exit Extended Diagnostic Mode and enter normal operating mode.

INITIALIZE (15)

This selection will initialize all of the MPX 110 system parameters to their factory default settings.

When selected, the Binary LED's will read the following:

Edit	**Bypass**	**Store**	**Tap**
O	O	O	●
MSB			**LSB**

Pressing the **STORE** button will execute the test.

When this selection is executed the remaining buttons, encoders, ADC Pots and footswitches (2) are inactive. The MPX 110 will be reset, perform the power on diagnostic sequence, and enter normal operating mode.

Restoring Factory Settings

CAUTION, this Procedure will destroy any user settings or registers.

1. Power up the MPX 110, then press and hold the **Bypass**.
2. Turn VARIATION to **15**.
3. Press **Store**.
4. The MPX 110 will clear the registers then cycle through a normal power up and return to normal running mode

Disassembly/Reassembly

DISASSEMBY

1. Remove six-(6) screws from the housing: three-(3) from the top, and three-(3) from the bottom.
2. Carefully remove the two end caps, swinging them out by the rack ears.
3. Remove five-(5) plastic nuts from the jacks on the rear panel.
4. Remove the two-(2) small Phillips head screws at the rear panel MIDI jacks.
5. Holding the front panel, carefully remove the cover.
6. To disconnect the circuit board from the front panel:
   6.1. Pull off the seven-(7) knobs on the front panel
   6.2. Remove the seven-(7) nuts and washers from the front panel.
   6.3. Hold the unit face down, and carefully separate the circuit board assembly from the front panel.
   6.4. Carefully remove the buttons from the rear of the front panel.

NOTE: The buttons are loose and can fall out.

REASSEMBLY

1. Holding the front panel face down, reinsert the buttons. Continue to hold the front panel face down so as not to loosen the buttons.
2. From the rear, carefully position the circuit board and insert it into the front panel.
3. Replace the nut and washer on one potentiometer at each end and hand tighten.
4. Replace the remaining potentiometer nuts and washers. Check for alignment, then tighten all nuts. Do not overtighten.
5. Replace the cover, being careful to align the jacks and power connector with the holes in the rear of the cover.
6. Replace the seven-(7) plastic nuts on the jacks. Be careful not to overtighten.
7. Replace the seven-(7) knobs on the front panel.
8. Replace the two-(2) screws at the rear panel MIDI jacks.
9. Insert the two end caps by hooking the rear tab of each into each end of the cover.
10. Holding the end caps in place, install the six-(6) screws.
11. Tighten the rear-panel screws next to the power connector.

REMOVAL AND INSTALLATION OF COMPONENTS

From time to time, it may be necessary to replace pots, jacks or other components. When desoldering, be careful not to overheat the board. Use all caution to prevent damage to the circuit board, traces and pads. When installing pots, jacks or displays, make sure that they are mechanically flush with the circuit board prior to soldering in place. If not properly aligned, stress can be placed on the new components and the board, resulting in early failure of the board and/or component.

Chapter 6 Theory of Operation

SCHEMATIC WALK-THROUGH

Sheet 1:

This sheet shows the analog input section (U21-23), and the analog output section (U17 & U18) and their associated circuitry.

INPUT STAGE

Separate unbalanced 1/4" phone jacks (J8 and J9) are provided for left and right input signals. A single input source will be routed to both left and right input stages if only the right input (J9) is used. J8 and J9 also provide chassis ground through an integrated ground lug from the PCB to the cover.

Capacitors (C81 and C85) are found at the inputs to prevent unwanted high frequency interference from entering or leaving MPX 110 through the input cables.

DC blocking is incorporated by capacitors (C80 and C84) in line with the signal path.

The input impedance of the MPX 110 is set by R86 and R99, 1M Ohm per channel and 500K Ohm when sum-to-mono by plugging in the Right I/P only. This allows the MPX 110 to be used with a wide variety of input sources including electric guitars. However, this high impedance makes the input susceptible to noise pickup. For this reason the left and right inputs short to ground when empty.

D16 and D17 protect U21 and U23 from being destroyed by potentials > |5V|. R87 and R100 limit the current through D16 and D17 during conduction to protect them. This insures signals at the input of the U21 and U23 are never greater than 0.7V above the op-amp rails.

The non-inverting inputs of one half U21 and U23 are used as the signal input buffer to maintain a high input impedance, provide unity gain at low frequencies, and pre-emphasis.

R88, R89, C89 and R101, R102, C101 are feedback networks around U21 and U23 respectively. They form a high pass shelf for pre-emphasis. It is a 10-dB shelf starting at 3 kHz and ending at 9 kHz. This is 15/50uS curve with matching de-emphasis on the output. The pre/de-emphasis improves the SNR of the unit. Capacitors C91, C103 provide high frequency compensation for this input buffer stage.

C94 and C106 remove offset so potentiometer wiper noise in R92 is eliminated. R92 is a ganged dual pot for input level control.

The second half of U21 and U23 is a gain stage, which provides approximately 25db of gain. R90, R91 and R103, R104 set the gain of the respective channels. C95 and C107 are used for op-amp compensation at high frequencies.

IN_LEFT and IN_RIGHT are passed on to Sheet 2 for further signal conditioning.

OUTPUT STAGE

OUT_LEFT and OUT_RIGHT come in from Sheet 2. Two analog switches (U17) provide output muting during power up and power down conditions. MUTE/, pins 9 and 10 of U17, control these switches and are low on power reset. When MUTE/ is low, pins 4 and 5 of U17 are connected for the right output and pins 15 and 2 of U17 are connected for the left output, creating a low impedance signal path to ground. These switches are place in parallel with the output level potentiometer before the output stage. Approximately 43db of attenuation is achieved when the switch is on (MUTE/ is low).

A dual op amp (U18) and its associated circuitry (R54, R55, C60 and R56, R57, C61) make up the final output stage. This stage provides 10.5db of gain and the complimentary de-emphasis curve to compensate

for the pre-emphasis function performed before the conversion process. C59 and C62 are the +V and -V power supply bypass capacitors for U18.

An impedance of 75 Ohms is developed by R52 and R53 for the left and right outputs respectively. These resistors also provide current limiting protection. The output 1/4" unbalanced phone jacks (J6 and J7) are configured in such a way that, when only the right jack (J7) is connected, the left and right outputs are summed together to provide a mono output. The left jack (J6) can support stereo headphones if the right jack is not connected. The left channel appears on the tip and the right channel appears on the ring of a stereo phone plug of this three-conductor 1/4" phone jack. C55 and C56 are provided for RFI suppression at the outputs.

Although the output op amp can drive high-impedance (>100 Ohms) headphones, it is not designed for low impedance headphones. For best results, use a headphone amp.

Sheet 2

This sheet shows the CODEC device (U19), the input signal DC bias circuitry (R78 and R79), the single-ended to differential input amplifiers (U22), and the differential to single ended output amplifiers (U20). Shown also are the various clock and control signals used by the CODEC.

SINGLE-ENDED TO DIFFERENTIAL CONVERTER

Each section of dual op-amp U22 is a unity gain-inverting amplifier. R84 and R85 fix gains at 0dB for the left channel and R97 and R98 for the right channel. The non-inverting inputs of each amplifier are tied to analog ground, creating a virtual ground at the junctions of the input and feedback resistors for each channel. Signals IN_ LEFT and IN_ RIGHT from the previous page are AC coupled into these amplifiers by C90 and C102. Each phase of the differential output signal pairs are impedance balanced via R82/R83 for the left channel and R95/R96 for the right, and then AC coupled via C86/C87 and C96/C97 respectively. Each phase of the differential signal pairs are then DC biased via the resistors R80/R81 and R93/R94. This DC bias of 2.94V is provided by a resistive divider comprised of R78 and R79 while C82 and C83 de-couple this bias voltage to remove ripple and noise. Because the CODEC samples the input at 256fs, R82/R83/C65 and R95/R96/C66 form low pass filters. C86, C87, C96, and C97 simply provide AC coupling into the CODEC.

AK4528 CODEC

The AKM CODEC AK4528 is a high performance 24-bit A/D-D/A device, which performs anti-alias filtering, analog to digital conversion, and digital to analog conversion. Although it supports digital 15/50uS de-emphasis and sampling rates up to 96kHz, the MPX110 uses analog de-emphasis and 44.1kHz sampling. Digital de-emphasis is hardwired OFF (DEM0 =1, DEM1=0).

The Codec AINL/R inputs are fully differential. The input signal range is scaled to the VREF pin. Nominally, this range is defined as (0.56 x VREF) Volts peak to peak. With VREF equal to 5V and a DC input offset voltage of 2.9V The output code of the ADC is 0x7FFFFF positive full scale and 0x800000 negative full scale. The data is in 2’s complement form. The input is sampled at 64fs (2.8224 MHz with fs = 44.1kHz). Serial data is clocked in on the rising edge of the bit clock and is aligned with the second bit clock following the leading edge of each transition in the LRCLK (FS). This alignment is determined by setting the serial data interface pins to support the I2S format. The Lexichip3 receive port (SDIN0) is configured to support this format.

During power up and power down, the ADC, DAC, digital filters, and control registers are reset by signal PWR_DN/. This is an active low signal and is provided by a latch, U2 (4C7). The CODEC is brought out of power down mode when the Z80 writes ZD6=1 to Lexichip bit map address (xB2E) ZREG2/ latching PWR_DN high and the ADC and DAC initializes after a period of LEX_256FS.

The CODEC is constantly making ADC conversions of the AINL/R signals and output them in I2S format on pin 13 SDTO, or A/D_DATA to the Lexichip (3B6). Similarly, the CODEC takes the D/A_DATA from the Lexichip in on pin 14 SDTI in I2S format and the DAT presents balanced analog outputs at AOUTL/R+/-. A quick test of A/D and D/A integrity can be accomplished by removing R59, lifting U19pin14 and connecting U19p13 and U19p14. This bypasses all of the digital processing of the Z80 and Lexichip. In this configuration, a sine wave on the input will equal the sin wave on the output with very little distortion. If there is distortion or no signal out, then you know the problem is in the analog circuit. If this works fine, then you know the problem is in the digital circuitry. (Of course, the effects' processing is out of the circuit in this mode.) Remember to remove jumper from p13-p14 and reinstall R59 when you have completed the test. C63 and C64 provide power supply de-coupling of the analog supply line and voltage reference of the AK4528 while C69 de-couples the digital supply line and output buffer supply pins. R60 DC couples the analog and digital supplies together while providing a measure of isolation of digital switching currents from leaking back into the analog supply.

C67 and C68 de-couple the VCOM pin of the CODEC. This pin is the bias voltage of the ADC inputs and the DAC outputs; this voltage is equal to VA/2.

DIFFERENTIAL TO SINGLE-ENDED OUTPUT AMPLIFIERS

The analog outputs of the CODEC are full differential with a full-scale swing of (0.54 x VREF) volts peak to peak. This output signal is centered on 2.5V. Both sections of dual op amp U20 are configured as unity gain second order low pass filters with an Fc = 93.2kHz. These filters provide summing of the differential signals for each channel into single-ended signals. R70, R72-R76, C77-C79 comprise the low pass filter for the left channel (OUT_LEFT) while R61,R64-R68, C70-C72 form the low pass filter for the right channel (OUT_RIGHT). Both signals are referred back to page 1 to the Output and Mute circuitry. Regulated +/-5V rails power these op amps.

Sheet 3

Lexichip-3B (U11) is a Lexicon proprietary audio DSP (digital signal processor) ASIC (application specific IC). The L3 has multiple functions: I/O processing, clock generation, sample management (DSP).

L3 INITIALIZATION

Configuration pull ups and pull downs, RP2, RP9 (10K resistor networks) set the operating mode of the Lexichip3 via the data bus ZD[7:0] when the RESET/ is released. The pull up/down value follows:

	ZD Bits				
	7	**6**	**5**	**4:2**	**1:0**
Value	0	0	0	010	00
Function	CHIP_TRST	EXTMCX	EXTM	ZCLKSEL	HADEC

CHIP_TRST: The unidirectional output buffers are enabled for normal operation.
EXTMCX2: Source MCX2 (8X XTAL Frequency) from internal PLL..
EXTMC: Generate MC (Masterclock) Internally.
ZCLKSEL: Z80 ZCLK = PLL Clock Divided by 10 (ZCLK clock-tree output).
HADEC: Select Z80 Address Map 0 (More details below).

ADDRESS MAP 0
0000 - 3FFF 16K Common ROM (ZDEC0/)
4000 - 4BFF 3K Lexichip3 Internal Decodes*
4C00 - 4FFF 1K Expansion Area (ZDEC2/)
5000 - 5FFF 4K Common SRAM (ZDEC1/) (* note 3)
6000 - 7FFF 8K Bank-Swapped SRAM (1-16 Banks, 8KB - 128KB) (ZDEC1/)
8000 - FFFF 32K Bank-Swapped ROM (1-16 Banks, 32KB - 512KB) (ZDEC0/)

Upon the rising edge of RESET/, the Lexichip 3 reads ZD[7:0]. However, if the Z80 reset was the same signal as the L3 reset, then the L3 would never see the configuration resistors, since the Z80 would have

activity on the ZD bus. So, the Z80 and the L3 have separate resets (ZRST/ and RESET/ respectively). When the Z80 comes up in reset, it will have indeterminate data on the bus. The Z80 needs some clock cycle while in reset to drive its data bus to hi-Z. This explains the need for circuitry U6 and U7, R32, and C24 (4B7). It provides separate reset and clocks to the Z80 so it can set its data bus to hi-Z while in reset and stay reset while the L3 comes out of reset and reads the configuration resistors.

R68, R76, and C67 form a reference network for the PLL. R73 and R74 provide weak pull-ups for SP_MASTER/ and SPDIF_OUT respectively. R92 and R100 provide weak pull-downs for MUTE/ and DE_EMPH/ respectively. These pull-down components ensure that these signals default to their active states during power up. Resistors R69, R70, R71, and R77 provide RFI protection by slowing down the edge rates of LEX_FS/, D/A_DATA, LEX_64FS/, and LEX_256FS respectively. R72 is a provision for further RFI protection. Currently all that is required is for this component to be a 0-ohm resistor. R75 provides a DC coupled power source to the internal PLL on the Lexichip3. C68 and C69 de-couple this supply line.

AUDIO MEMORY

The audio memory for the Lexichip3 is provided by 1Mx16 DRAM (U10). However, the MPX110 only uses 8 of the available 16 data bits, with the most significant byte pulled up by RP5-RP6 Effectively this DRAM is being used as a 1Mx8 device. The address bus and memory control signals provided by the Lexichip3 are series terminated by resistors R93 through R98 and R101 through R107. This is done to provide RFI protection. Since the most active signals on this bus are LEX_A0 and LEX_A1, these are the ones that will cause the most emission, therefore R93 and R101 are set to 180 ohms; this value effectively slows down the edge rates of these two signals. The remaining bus signals (LEX_A[2:9]) are less active and therefore do not require edge rate reduction; R94, R96 through R98, R102, R105 and R106 are set to 0 ohms. Control signals CAS/, RAS/ and WE/ require edge rate reduction due to their high level of activity. Therefore, R95, R103, and R104 are 180 ohms.

MASTER CLOCK GENERATOR

Y1, C76, C77, and R91 comprise the master clock generator. Signal LEX_256FS is equal to the frequency generated here (11.2896MHz). Pins 74 and 75 on the Lexichip3 are essentially the output and input of a CMOS buffer, respectively.

I/O

The L3 is used in many Lexicon products and provides most of the I/O needed by embedded systems like the MPX-110. Looking over the L3 you will find pins designated “PIOA” and “PIOB”. These are programmable pins for I/O. For example: pin 95, “PIOB_2” controls “SWITCH ROW0” and pin 31, “PIOA_5” controls “SWITCH ROW1”. These I/O pins latch the state of the “TAP”, “BYPASS”, and “STORE” switches (7/B2). The Z80 sets up the L3 I/O direction register and reads or writes to the port register in order to get or provide peripheral device information. The L3 registers are addressed with signals ZA[15:0], read or written to with ZD[7:0] and controlled by ZCTRL.

The Z80 also uses the L3 to store system parameters when the MPX-110 is shutdown. Parameters like, Global tempo and the tap status. The serial eeprom, SEEPROM (U12) is clocked by “PIOB_5” pin96 and data stored or retrieved by “PIOB_4” pin 98.

SEEPROM

Non-volatile data storage is incorporated with a 2 wire serial/I2C 24C32 (32K bit). This serial EEPROM (U12) uses a two-wire bus protocol. U12, pin 5 is the serial address/data input/output, this is a bi-directional pin used to transfer addresses and data into and out of the device. U12, pin 6 is the serial clock input used to synchronize the data transfer to and from the device.

Currently pins 98 and 96 of Lexichip 3 are configured as PIOB (7) and PIOB (4). PIOB (7)(pin 96) is used to generate the serial clock and PIOB (4)(pin 98) is the bi-directional address/data for the EEPROM.

EEPROM_DATA is pulled high through RP10, this signal must remain in a high logic state, this is so the EEPROM SDA signal can pull this signal to a low logic level to generate an acknowledge pulse after the reception of each byte.

Z80 MEMORY MANAGEMENT

Note that all address decoding RAM_EN/, ROM_EN/, ROM_A15/A16 is done within the Lexichip3. These signals select Z80 access from ROM (code), RAM (parameters and variables) and ROM A15/A16 (bank switching).

CLOCKS

This chip mode determines various system parameters: Host address decode map, masterclock frequency and source, and zclock frequency and source. Given the desire to have an audio sample rate of 44.1KHz, the Lexichip 3 crystal input is selected as 11.2896 MHz, the internal PLL bumps this up 4X to a Lexichip 3 master clock frequency of 45.1584 MHz. All other clocks, including ZCLK/ are derived from this Lexichip 3 master clock. The conversion clocks, FS, 64FS, and 256FS are derived from the 11.2896 MHz xtal. Notice the Z80 is multiplexed clocks through U6p5&6 (4B7). U7 clocks while in reset, then ZCLK from L3 once L3 is initialized.

DSP

L3 takes samples at word clock rate from the Codec in I2S format on A/D_DATA. L3 converts I2S to byte audio data and puts it out to the audio data memory U10, a 1Mx16 DRAM. The L3 is setup pass 1 byte/cycle to the DRAM or 3x8 to pass the 24bit sample (LXD [7:0]). Since the DRAM part has a 16bit data bus, the high 8 bits are pulled high with resistor packs RP5&6. Once the data is stored in the DRAM, the L3 will store pointers (taps) and process up to 255 steps per word clock. The DSP function will add historical samples from the taps to current samples according to the algorithm for the effect. The combined samples

Sheet 4:
The Z80 (U8), ROM (U4), SRAM (U5, incoming encoder buffer (U9), and outgoing latch (U2) represent the MPX110 microprocessor control circuits. The Z80 and the L3 interact regularly to control the processing. For example, when the Z80 passes data to the memory map address for ZREG2/ the data will be latched on U2 by the clk signal CLT_REG/ generated by the Lexichip. Similarly, when the Z80 reads from the memory map address for ZDEC2/, the L3 will generate ENC_READ/ which passes data to the Z80 data bus via U9. U6, multiplexes init clocks and reset with ZCLK and ZRST from the L3.

The L3 also selects code and data space for the Z80 with signals ROM_EN/ and RAM_EN/. Further, the ROM is banked switched with signals ROM_A15 and ROM_A16. This allows block of 32KB to be selected.

The 128kx8, 27c010, OTP EPROM, U4) holds the boot and the application code.

Running the Z80 at 9.0316MHz and using the zero wait states for ROM access we can accommodate a ROM with an access time of 112nS or better. By inserting one wait state we can use a ROM with an access time of 223nS or better.

8K x 8 SRAM (U5) can have a relatively slow access time, 80ns, and faster will operate with one wait state with the Z80 running at 9 MHz.

Z80 RESET

In order to guaranty the data bus is tri-stated when the Lexichip 3 is released from reset, the Z80 must have a clock present at its ZCLK input when the Z80 released from reset. This is accomplished by using a 74VCTT14 (U7), along with C24 (10pf) and R32 (47k) as a feedback oscillator. A 74HC157 (U6) is used to select the ZCLK source from either the U7 oscillator or the Lexichip 3, and also gates the reset signal for the Z80 during reset.

During power up while RESET/ is asserted low, bringing U7 pin 1 high enables the feedback oscillator. The oscillator's output is selected as the ZCLK, and ZRST is held low by U6.

When the RESET/ signal goes high, the feedback oscillator is disabled as U7 pin 1 is brought low, the ZCLK_LEXI3 clock (from the Lexichip 3) signal is selected as the ZCLK, and ZRST is controlled by ZRST_LEXI3 signal (from the Lexichip 3).

Sheet 5

ENCODERS

The rotary encoder is 16 position, 4 bits. Gray code is generated in the following clockwise rotation sequence (hexadecimal, terminals 1-4): 0,1,3,2,6,7,5,4,C,D,F,E,A,B,9,8. It is necessary to have pull-up resistors at the Front Panel encoders (SW3 and SW4). RP1 & RP3 pull up the inputs, this prevents Lexichip 3 inputs from floating and provides a default non-active switch state of logic high. ??

Sheet 6

CONTROL INPUT (IAD)

The pot A/D converter is the integrating type made from current source Q5 and 8-bit timer in the Lexichip 3. To start the conversion, the Z80 tells the Lexichip 3 to bring RESET_IAD high, which toggles U13 and discharges capacitor C44 to less than 0.2V. Next the Z80 selects which pot (ADMUXIN0 - 3) the Lexichip 3 will digitize. It does this by writing to a IAD mux register in the Lexichip 3.

The Lexichip 3 then starts its timer and brings RESET_IAD low. C44 starts to charge from the current source. Once the capacitor voltage exceeds the pot voltage, the muxed comparator output goes low. This produces a high level interrupt to the Z80, which disables the timer. At its convenience the Z80 reads the timer and derives the voltage on the pot. R44 sets input voltage range from 0-3V. This voltage is also the calibration voltage for the IAD, it will guaranty the pots full range will be used regardless of fluctuation in voltage and temperature.

Sheet 7:

FOOTSWITCH

Footswitch jack J2 use resistors (R9, R11) and capacitors (C8, C9) to filter out RFI. D10 and D11 help protect from over voltage or static shock and R12 and R10 provide a default non-active switch state of logic high.

LED/SWITCH MATRIX

There are eight discrete LED’s on the front panel, which are organized into 2 columns and 4 rows.

An octal D-Flop U2 clocks the data bus on the rising edge of CTL_REG/. ZD4 creates (COLUMN_STRB0) and ZD5 creates (COLUMN_STRB1). These column select lines are active low. These are buffered and inverted by switching transistors Q2 and Q3. When COLUMN_STRB0 line is driven low, net line “col0” is high and if DSPLY_ROW0 line is driven low, then LED D18 will light. In this configuration, if SW1 “TAP” switch is pressed, the SWITCH_ROW0 signal will go high. R28 pull down will hold the SWITCH_ROW0 signal to ground when the switch is not pressed.

Row lines are driven directly from U2 (sheet 4). U2 is only driving four lines, so the total current in the IC remains well below 100mA. The 100-330 Ohm resistors (R16-R19) limit the row current to about 28mA or less. The variance in resistor values is an adjustment for brightness.

Sheet 8:

POWER FAIL/RESET

Reset signaling is controlled by the +5UNREG voltage. If the +5UNREG voltage at the input of the +5VD regulator (U1) is high enough to create a 2 volt or greater drop across the regulator, then the differential between the voltage divider (R1 and R2) at the emitter of Q1, and the regulated +5VD at the base of Q1 will be enough to turn on Q1. As Q1 turns on, it charges C7 through R3. The voltage across R3 and R4 goes from 0V to about +6V. R3 is also used as a voltage divider to generate RESET/ at a 5V level taking Lexichip 3 out of reset. C7 is discharged through D5 on power down.

The MPX 110 power supply provides three regulated DC output voltages: +5VD for digital circuits, +5VA and -5VA for analog circuits.

AC power is provided by an external transformer rated at 9VAC @ 1.9A. The transformer output is terminated with a 5-mm/2.5-mm barrel type connector (J1), with its mating input jack located at the rear panel of MPX 110. A .1 uF capacitor, C1 is connected across the AC input to help prevent noise spikes from entering the unit. In addition, C2 (470pf) stop circuit generated RFI from radiating through the power line.

All three regulated supplies (+5VDC analog, -5VDC analog and +5VDC digital) consist of a single diode (D1, D2 and D3) used as a half wave rectifier to produce the unregulated 5 volt supply (approximately 10 VDC) across each supply's filter capacitor (C3, C4, and C5). The supplies are post-regulator filtered with 22 uF capacitors (C6, C50, C53). The +5VUNREG supply is monitored by the reset circuit for power up and power fail conditions.

Voltage regulation is handled by three TO-220 packaged ICs:

+5VD digital circuits - U1 (LM2940)
+5VA analog circuits - U15 (LM2940)
-5VA analog circuits - U16 (MC7905)

Current limiting and short circuit protection are incorporated into the internal circuitry of these ICs.

The MPX 110 power supply also provides two unregulated DC output voltages: +V and -V for the analog output stage at U18. The +V and -V power supplies were added to help isolate the output stage from the rest of the power supply, and to delay the turn-on during power up to minimize the power on thump characteristics at the analog output.

The unregulated +V supply (C49, C51, R46, R47 & Q6) and -V supply (C52, C54, R48, R49 & Q7) are both derived from capacitance multipliers which multiplies the value of the capacitor by the beta of the transistor for a higher (but poorly regulated) output voltage.

Twenty +5VD bypass caps, five +5VA bypass caps and five -5VA bypass caps are represented on page 8 of the schematic.

MIDI I/O

The MIDI interface utilized by MPX 110 complies with the MIDI specification. It incorporates 5 pin, female DIN connectors for input and output (J4 and J3). MIDI IN is opto-coupled for ground isolation through U3 to the UART (in Lexichip 3). The MIDI OUT signal is provided by Lexichip 3 and is fed to current loop driver Q4 and out J3. FB1 and FB2 are used to reduce RFI radiation.

S/PDIF OUT

The S/PDIF output signal is generated using a pair of 74VHCT14 gates U7. Each gate has to source about 6.25 mA??, well within its capabilities. The resistors are selected so that the voltage across R29 is 0.5Vpp,

assuming 75 Ohm load resistor across the S/PDIF connector and a Voh out of the gates of 4.7V, which typical Voh at 6mA.

C22 and C20 were added to the circuit to help meet RF compliance. However, they also band-limit the S/PDIF signal, which increases jitter. D13 helps protect from over voltage or static shock.

Chapter 7 Parts List

MPX110 MAIN BOARD ASSEMBLY

PART NO.	DESCRIPTION	QTY	EFFECTIVE	INACTIVE	REFERENCE
120-14142	ADHESIVE,EPOXY,THERM COND	0.00			U11
200-11946	POT,RTY,10KBX2,7MMFL,14,15L	3.00			R45,50,77
200-12169	POT,RTY,5K15AX2,7MMFL,14,15L	1.00			R92
200-12184	POT,RTY,10K15AX2,7MMFL,14,15L	1.00			R51
202-09794	RESSM,RO,0 OHM,0805	1.00			R58
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	3.00			R14,27,28
202-09871	RESSM,RO,5%,1/10W,1K OHM	3.00			R5,7,43
202-09894	RESSM,RO,5%,1/10W,1M OHM	3.00			R36,86,99
202-09897	RESSM,RO,5%,1/10W,470 0HM	2.00			R46,48
202-10466	RESSM,RO,5%,1/10W,20K OHM	4.00			R80,81,93,94
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	2.00			R9,11
202-10558	RESSM,RO,5%,1/10W,47K OHM	3.00			R10,12,32
202-10559	RESSM,RO,5%,1/10W,100 OHM	4.00			R38,59,87,100
202-10569	RESSM,RO,5%,1/10W,10 OHM	1.00			R39
202-10586	RESSM,RO,5%,1/4W,100 OHM	2.00			R16,17
202-10892	RESSM,RO,5%,1/10W,2K OHM	2.00			R47,49
202-11041	RESSM,RO,5%,1/10W,680 OHM	3.00			R6,8,35
202-11071	RESSM,RO,5%,1/4W,75 OHM	2.00			R52,53
202-11072	RESSM,RO,5%,1/4W,220 0HM	3.00			R13,15,21
202-11073	RESSM,RO,5%,1/4W,270 OHM	2.00			R18,22
202-11683	RESSM,RO,5%,1/10W,5.1 OHM	1.00			R60
202-12191	RESSM,RO,5%,1/4W,330 OHM	1.00			R19
202-12836	RESSM,RO,5%,1/10W,2.7K OHM	1.00			R33
202-14584	RESSM,RO,5%,1/10W,10K OHM,0603	3.00			R20,34,37
202-14585	RESSM,RO,0 OHM,0603	1.00			R23
203-10424	RESSM,RO,1%,1/10W,4.99K OHM	2.00			R54,56
203-10578	RESSM,RO,1%,1/10W,2.21K OHM	1.00			R44
203-10581	RESSM,RO,1%,1/10W,3.32K OHM	1.00			R78
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	2.00			R3,41
203-10840	RESSM,RO,1%,1/10W,750 OHM	2.00			R89,102
203-10894	RESSM,RO,1%,1/10W,340 OHM	4.00			R82,83,95,96
203-10895	RESSM,RO,1%,1/10W,681 OHM	1.00			R2
203-10896	RESSM,RO,1%,1/10W,1.00K OHM	1.00			R1
203-11075	RESSM,RO,1%,1/10W,95.3 OHM	1.00			R29
203-11079	RESSM,RO,1%,1/10W,715 OHM	2.00			R30,31
203-11083	RESSM,RO,1%,1/10W,49.9K OHM	1.00			R4
203-11723	RESSM,RO,1%,1/10W,4.75K OHM	13.00			R61,64,67,68,70 R72,75,76,79,84 R85,97,98
203-11734	RESSM,RO,1%,1/10W,4.32K OHM	2.00			R91,104
203-11996	RESSM,RO,1%,1/10W,6.49K OHM	1.00			R42
203-12167	RESSM,RO,1%,1/10W,374 OHM	2.00			R90,103
203-12198	RESSM,RO,1%,1/10W,2.15K OHM	2.00			R55,57
203-12199	RESSM,RO,1%,1/10W,316 OHM	2.00			R88,101
203-12478	RESSM,RO,1%,1/10W,68.1K OHM	1.00			R40
203-12491	RESSM,RO,1%,1/10W,205 OHM	4.00			R65,66,73,74
203-14566	RESSM,THIN,1%,1/10W,20.0K OHM	2.00			R63,71
205-14586	RESSM,NET,5%,ISOL,10KX4	9.00			RP1-3,5-10
205-14587	RESSM,NET,5%,ISOL,110X4	2.00			RP4,11
240-00609	CAP,ELEC,10uF,16V,20%,RAD	3.00			C7,49,52
240-00611	CAP,ELEC,22uF,16V,RAD	12.00			C63,73,74,83,86,87 C90,94,96,97,102,106
240-00614	CAP,ELEC,47uF,16V,20%,RAD	2.00			C51,54
240-06611	CAP,ELEC,1000uF,25V,20%,RAD	1.00			C3
240-09541	CAP,ELEC,3300uF,16V,20%,RAD	1.00			C5
240-11827	CAPSM,ELEC,10uF,16V,20%	1.00			C41
240-12330	CAPSM,ELEC,2.2uF,35V,20%	1.00			C68
240-12848	CAP,ELEC,3300uF,16V,20%,RAD	1.00			C4
241-00654	CAP,TANT,22uF,16V,RAD	3.00			C6,50,53
244-00661	CAP,MYL,.047uF,5%,RAD,BOX	2.00			C89,101
244-06883	CAP,MYL,.01uF,100V,RAD,5%	1.00			C44
244-09390	CAP,MYL,.01uF,RAD,5%,MINI	2.00			C60,61

244-10423	CAP,MYL,.22uF,50V,RAD,5%,BOX	2.00			C80,84
244-14616	CAP,MYL,3300pF,100V,RAD,5%,BOX	2.00			C70,79
245-09291	CAPSM,CER,470pF,50V,COG,5%	5.00			C2,71,72,77,78
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	1.00			C22
245-09895	CAPSM,CER,10pF,50V,COG,10%	3.00			C24,95,107
245-10416	CAPSM,CER,1000pF,50V,COG,5%	1.00			C25
245-10561	CAPSM,CER,100pF,50V,COG,5%	7.00			C10-12,88,91,100,103
245-10562	CAPSM,CER,150pF,50V,COG,10%	6.00			C8,9,55,56,81,85
245-10976	CAPSM,CER,47pF,50V,COG,5%	1.00			C20
245-11625	CAPSM,CER,33pF,50V,COG,5%	2.00			C37,38
245-11949	CAPSM,CER,1500pF,50V,COG,5%	2.00			C65,66
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	26.00			C1,14,21,31,34,43 C45-48,57-59,62,64 C67,69,75,76,82,92 C93,98,99,104,105
245-14588	CAPSM,CER,.01uF,25V,X7R,10%,06	19.00			C13,15-19,23,26-30 C32,33,35,36,39,40 C42
270-11545	FERRITESM,CHIP,600 OHM,0805	2.00			FB1,2
300-10509	DIODESM,1N914,SOT23	3.00			D6,8,12
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	6.00			D5,10,11,13,16,17
300-11599	DIODESM,GP,1N4002,MELF	4.00			D1-4
310-01007	TRANSISTOR,2N3904	1.00			Q6
310-01008	TRANSISTOR,2N3906	1.00			Q7
310-10422	TRANSISTORSM,2N4403,SOT23	2.00			Q2,3
310-10510	TRANSISTORSM,2N3904,SOT23	1.00			Q4
310-10565	TRANSISTORSM,2N3906,SOT23	2.00			Q1,5
330-10535	ICSM,DIGITAL,74AC273,SOIC	1.00			U2
330-11990	ICSM,LEXICHIP3B,100PIN,PQFP	1.00			U11
330-12452	ICSM,DIGITAL,74VHCT244,SOIC	1.00			U9
330-12845	ICSM,DIGITAL,74HC157,SOIC	1.00			U6
330-14642	ICSM,DIGITAL,74VHCT14,SOIC	1.00			U7
340-10877	ICSM,LIN,4556,DUAL OP AMP,SOIC	1.00			U18
340-11573	ICSM,LIN,NJM4580,DUALOPAMP,SOP	4.00			U20-23
340-11576	ICSM,LIN,7905,-5V REG,TO263	1.00			U16
340-11948	ICSM,LIN,LM339,QUAD COMP,SOIC	1.00			U14
340-12849	ICSM,LIN,LM2940,5V REG,TO263	2.00			U1,15
346-10508	ICSM,SS SWITCH,74HC4053,SOIC	2.00			U13,17
350-10545	ICSM,SRAM,8KX8,80NS,SOIC,50uA	1.00			U5
350-12637	ICSM,DRAM,1MX16,70NS,SOJ	1.00			U10
350-14158	ICSM,EEPROM,24C32,32K,SER,SOIC	1.00			U12
350-14759	ICSM,ROM,27C010,MPX110,V1.00	1.00			U4
355-12045	ICSM,CODEC,AK4528,24B,96k,VSOP	1.00			U19
365-09883	ICSM,uPROC,Z80,CMOS,10MHz,QFP	1.00			U8
375-02247	IC,OPTO-ISOLATOR,6N138	1.00			U3
390-09781	CRYSTAL,11.2896MHz	1.00			Y1
430-11938	LED,T1,GRN,PCRA,BLOCK	4.00			D7,9,14,15
430-11939	LED,DUAL,T1,GRN/RED,PCRA,BLOCK	2.00			D18,19
452-14617	SW,RTY,ENC,16POS,4BIT,GRY,20MM	2.00			SW3,4
453-12165	SW,PBM,1P1T,7MMSQ,250GF,PCRA	3.00			SW1,2,5
510-06042	CONN,DC POWER,PC,DJ005,2.5MM	1.00			J1
510-09790	CONN,DIN,5FC@180DEG,PCRA,SHLD	2.00			J3,4
510-10555	CONN,RCA,PCRA,1FCG,YEL	1.00			J5
510-11087	1/4"PH JACK,PCRA,3C,SW-TR,G,FT	2.00			J2,6
510-11548	1/4"PH JACK,PCRA,2C,SW-T,G,FT	3.00			J7-9
704-14132	HEATSINK,TO220,.75X.5X.5"H	1.00			U11
710-14560	PC BD,MAIN,MPX110	1.00		12/14/01	REV 1 PC BOARD
710-14560	PC BD,MAIN,MPX110	1.000	12/14/01		REV 2 PC BOARD
740-11287	LABEL,S/N,PCB,PRINTED	1.00			

MPX110 MECHANICAL ASSEMBLY

550-11929	KNOB,.69D,6MM/FL,BLK,LINE	5.00			
550-11930	KNOB,.85D,6MM/FL,BLK,LINE	2.00			
550-11931	BUTTON,.24X.64,BLK,W/LT PIPE	3.00			
635-12192	SPCR,4-40X1/2,3/16HEX,AL	1.00			PCB/BRKT TO FP
640-02812	SCRW,4-40X3/8,PNH,PH,BLK	2.00			CVR TO FRONT PAN
641-10989	SCRW,TAP,AB,4X3/8,PNH,PH,BZ	4.00			CVR TO SIDE PAN
641-12759	SCRW,TAP,AB,#2X1/4,PNH,PH,BZ	2.00			DIN CONN
644-14556	WSHR,SPG,.331IDX.622OD,.006THK	1.00			RCA CONN

650-03970	POPRVT,1/8X1/8,REG PROT HD,SS	1.00		BRACKET TO PCB
700-14962	COVER,MPX110	1.00		
701-11934	BRACKET,KEYSTONE,613,.147/.128	1.00		PCB TO FRONT PANEL
702-14641	PANEL,SIDE,1.71X3.93,ABS	2.00		
702-14960	PANEL,FRONT,MPX110	1.00		
740-09538	LABEL,S/N,CHASSIS,PRINTED	1.00		
740-13573	LABEL,MFR ID,.9X.25,SILVER	1.00		

MPX110 SHIP/PACKAGING MATERIAL

070-14956	GUIDE,USER,MPX110	1.00		
070-14957	NOTES,ERRATA,MPX110	1.00	06/01/02	
730-11670	INSERT,FOAM,ENDCAP,1UX4	2.00		
730-14964	BOX,DSPLY,24X7X4,MPX110	1.00		
750-14967	CD,LIT,MULTI-LANG,MPX110	1.00		

MPX110 TRANSFORMER OPTIONS

470-12754	XFORMER,PLUG-IN,120V,9VAC,1.9A	1.00		
470-12755	XFORMER,PLUG-IN,230V,9VAC,1.9A	1.00		

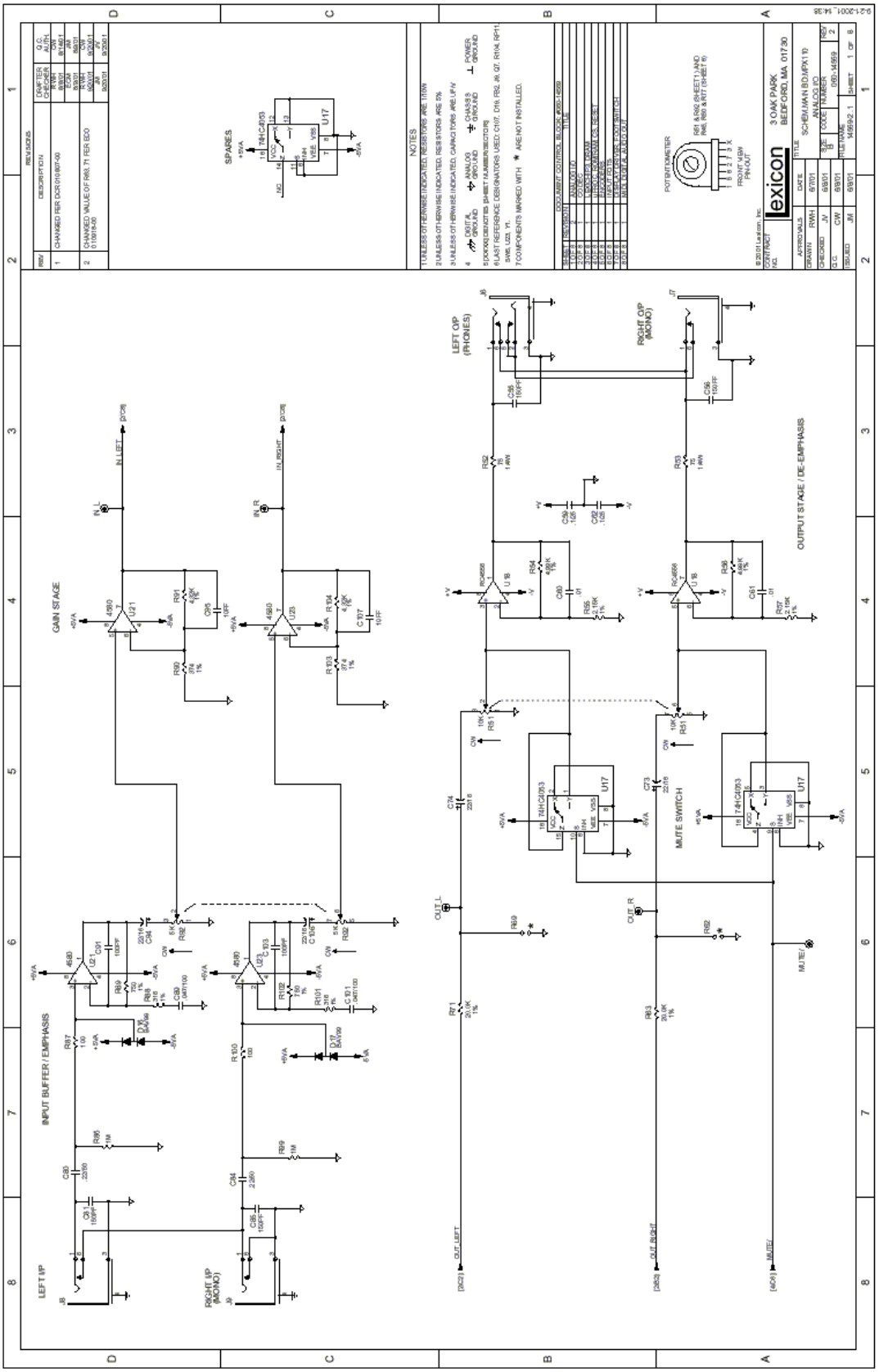
Chapter 8 Schematics and Drawings

Schematics:

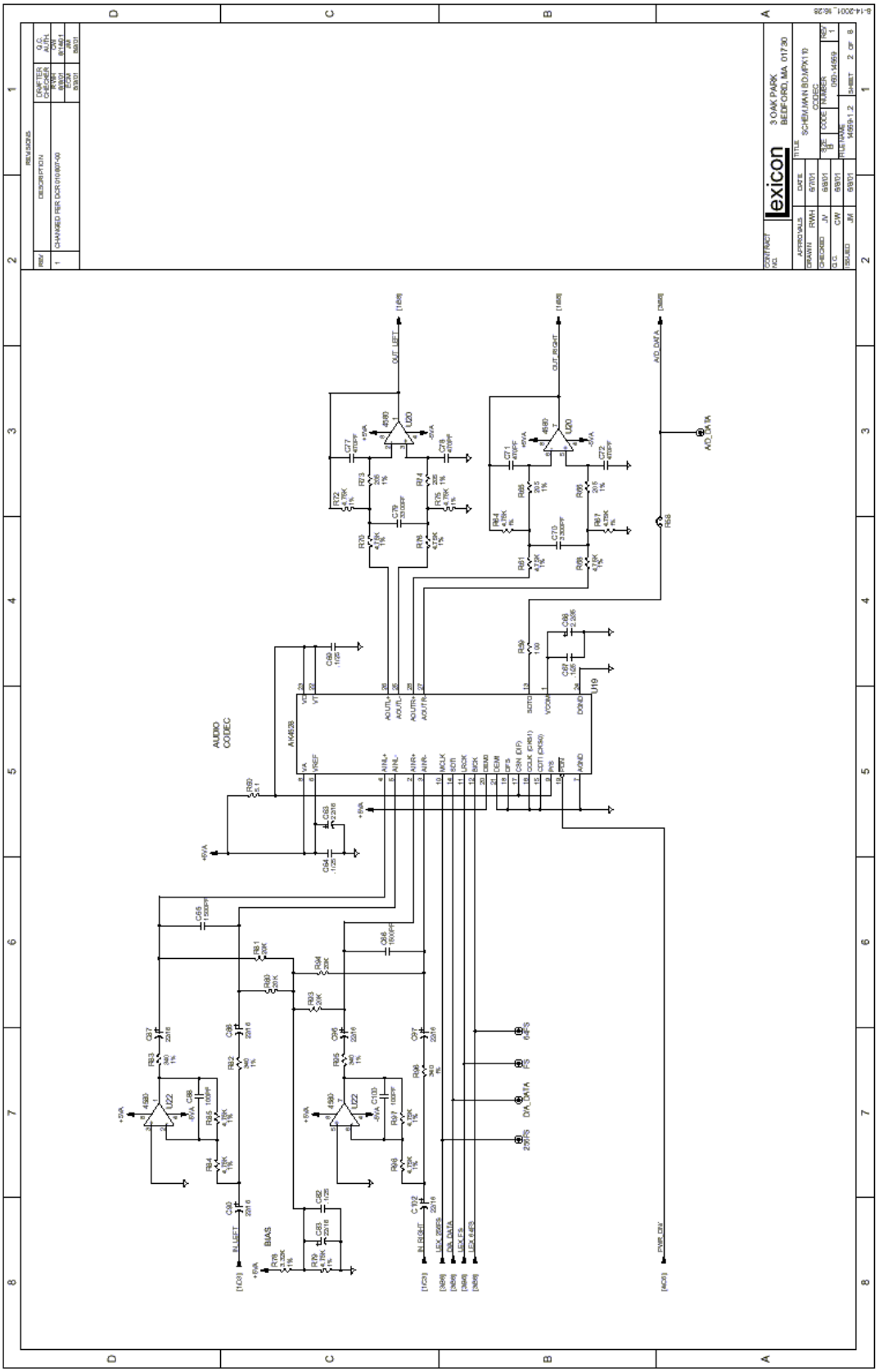
060-14569 SCHEM,MAIN BD,MPX110

Drawings:

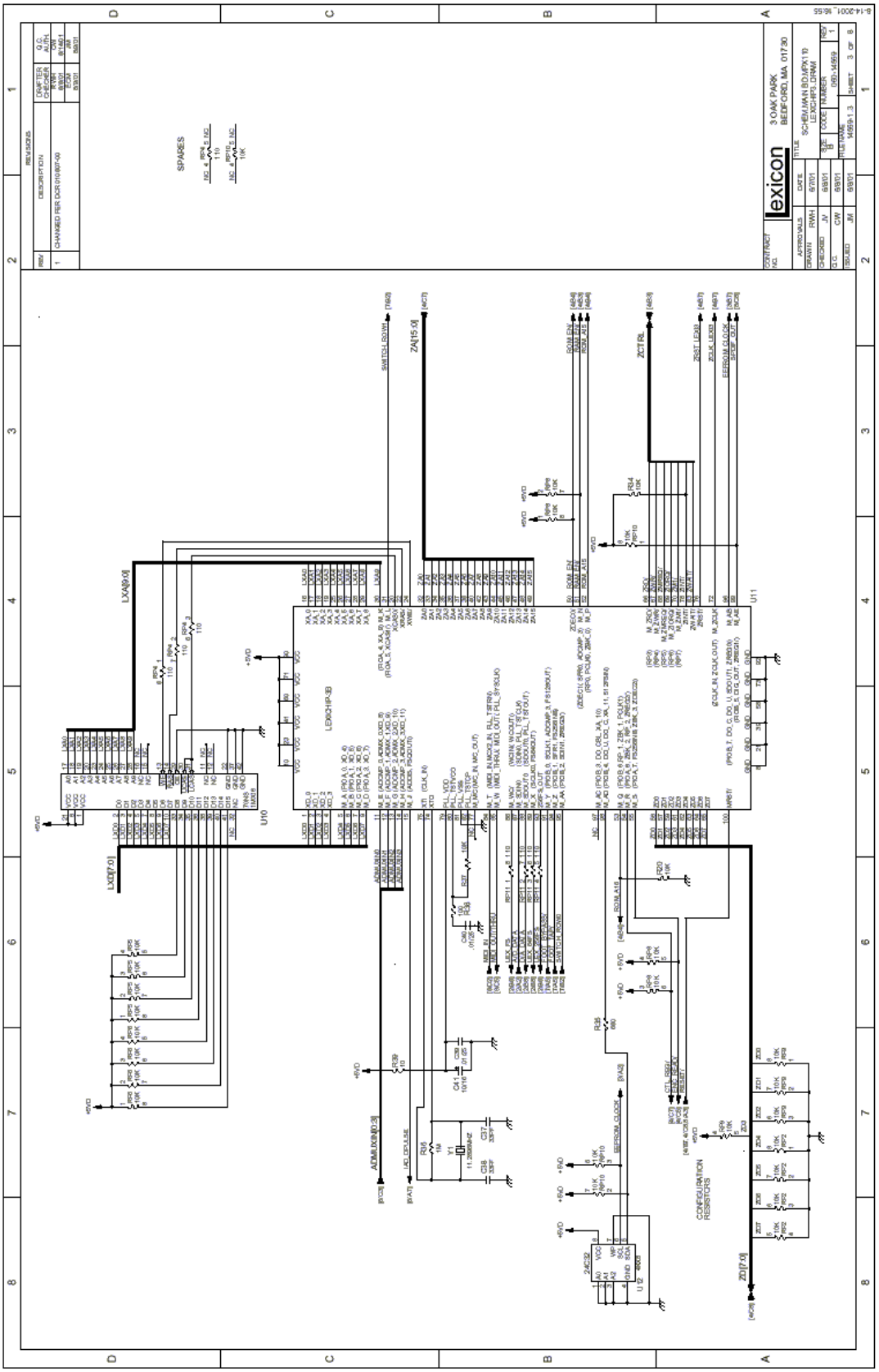
COMPONENT LAYOUT, MAIN BD,MPX110
080-14958 ASSY DWG,SHIPMENT,MPX110
080-14959 ASSY DWG,CHASSIS,MPX110



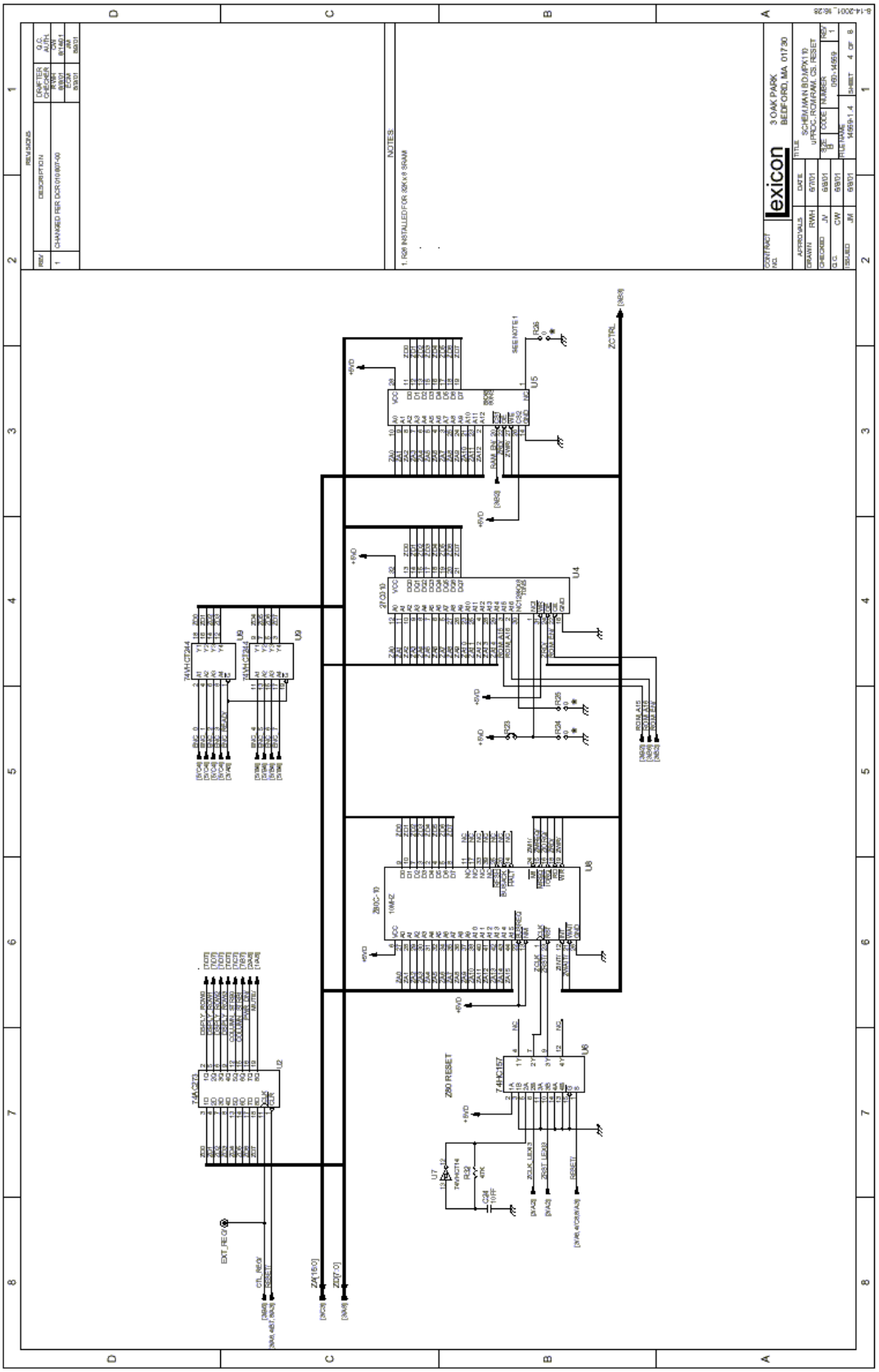
Your Notes:



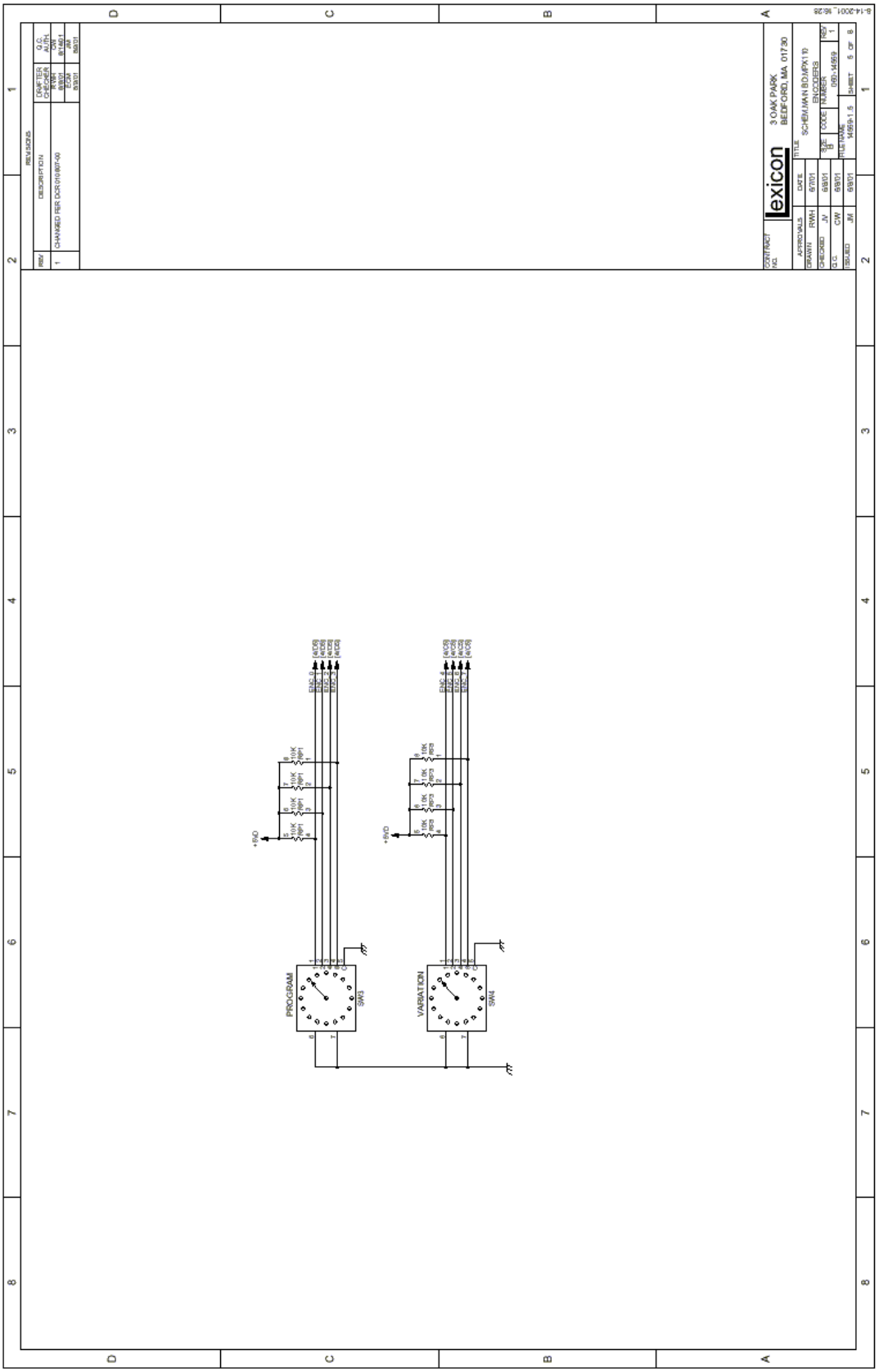
Your Notes:



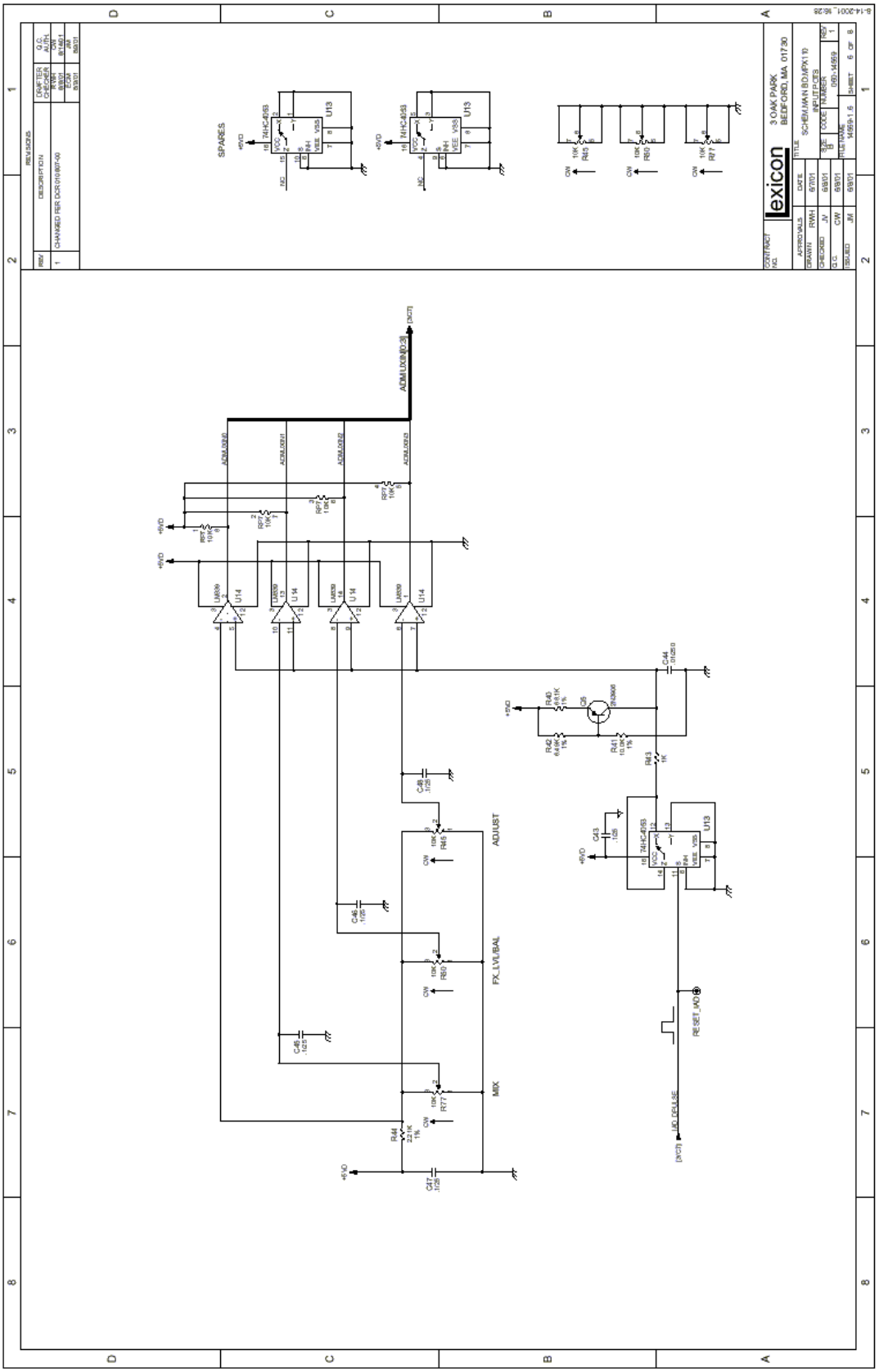
Your Notes:



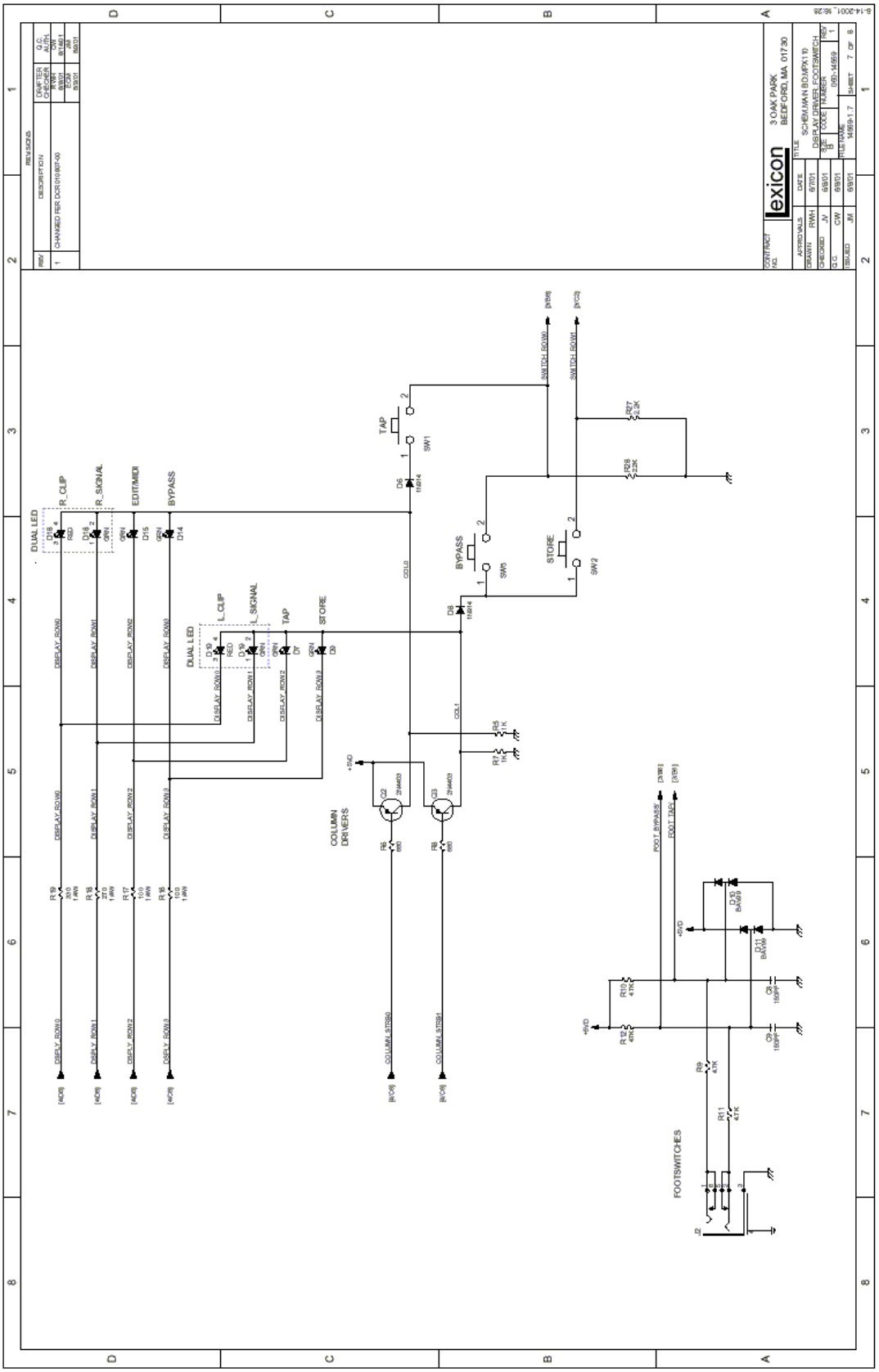
Your Notes:


PROGRAM
SW3
VARIATION
SW4
+5VD
+5VD
10K
10K
10K
10K
10K
10K
10K
10K
10K
10K
10K
10K
10K
10K
10K
10K
ENC A
ENC B
ENC C
ENC D
ENC E
ENC F
ENC G
ENC H
ENC A
ENC B
ENC C
ENC D
ENC E
ENC F
ENC G
ENC H

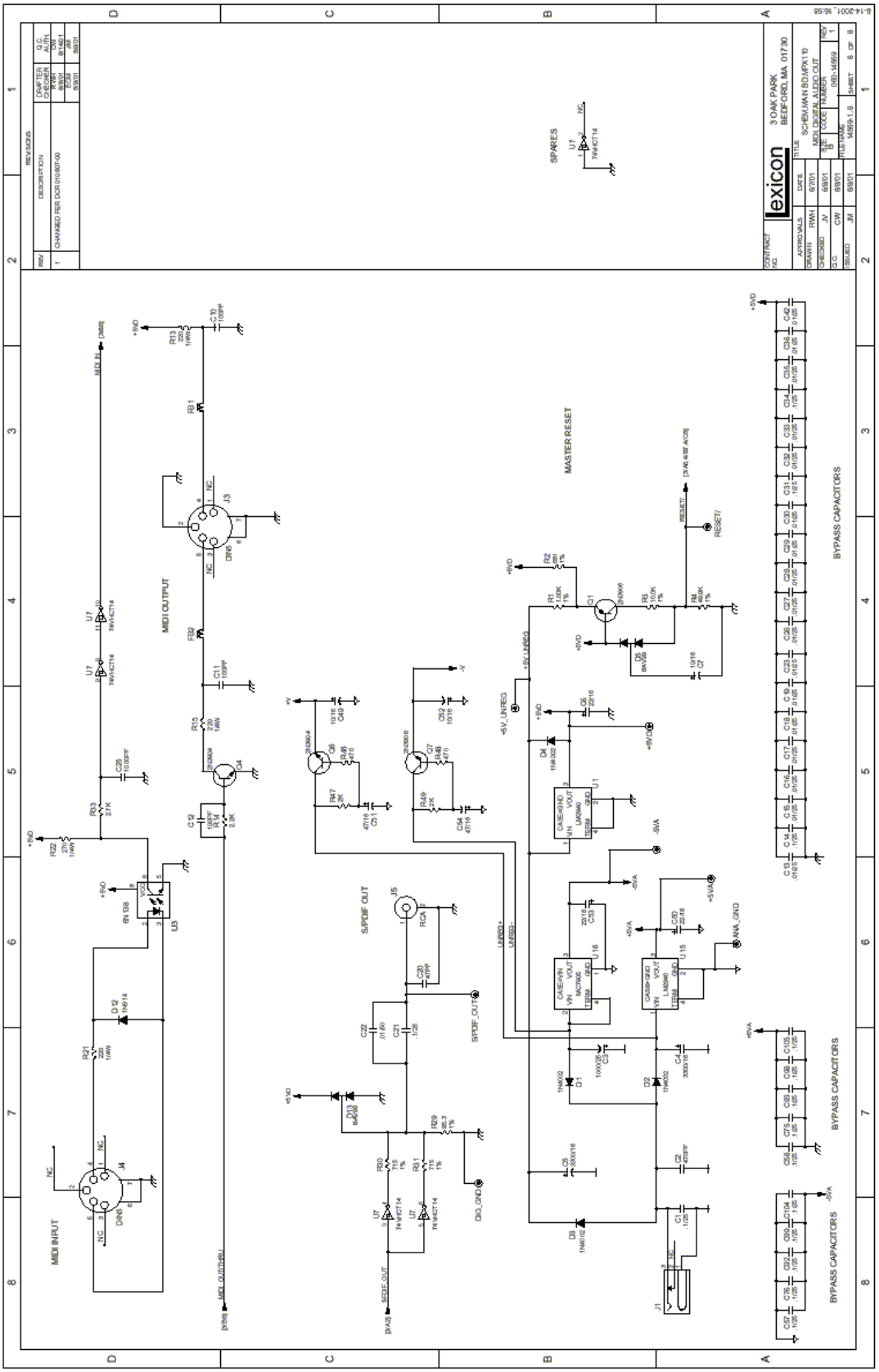
Your Notes:


lexicon
3 OAK PARK
BEDFORD, MA. 01730
SCHEMANN BOARD(PX110)
ADJUST
FX_LVL/BAL
MIX
RESET_IVD
SPARES

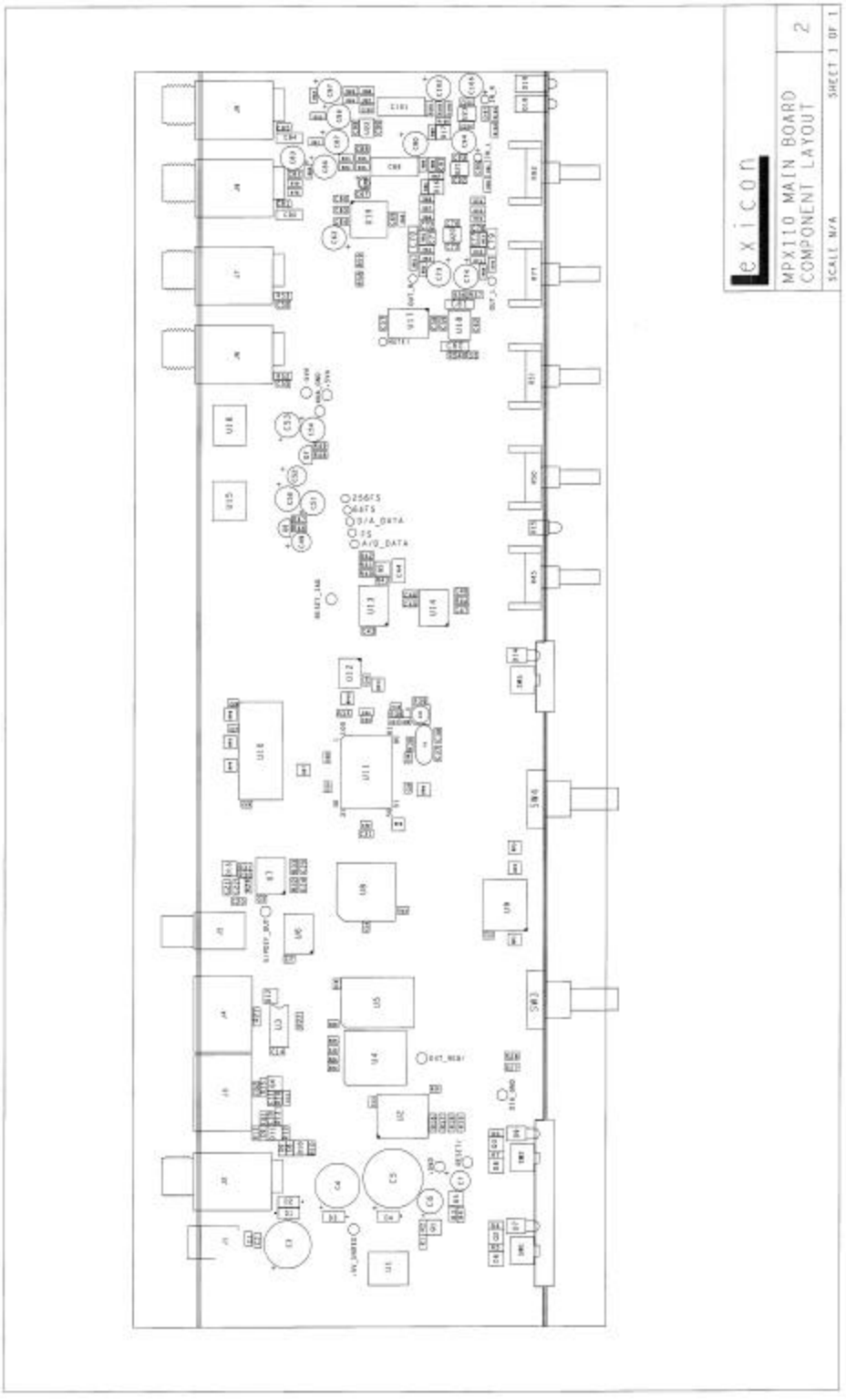
Your Notes:


lexicon
3 OAK PARK
BEDFORD, MA. 01730
SCHEMANN BOARD(X110)
DISPLAY DRIVER, FOOTSWITCH
DWG. NUMBER
065-14569
REV
1
SHEET 7 OF 8
DESCRIPTION
CHANGED PER DCR(10)(07-00)
DRAWN
CHECKED
ENGINEER
APPROVALS
DATE
R_CLIP
R_SIGNAL
EDIT/MIDI
BYPASS
L_CLIP
L_SIGNAL
TAP
STORE
DUAL LED
COLUMN DRIVERS
FOOTSWITCHES
FOOT_BYPASS
FOOT_TAP
SWITCH ROW0
SWITCH ROW1
DISPLAY_ROW0
DISPLAY_ROW1
DISPLAY_ROW2
DISPLAY_ROW3
COLUMN_STROBE
+5VD

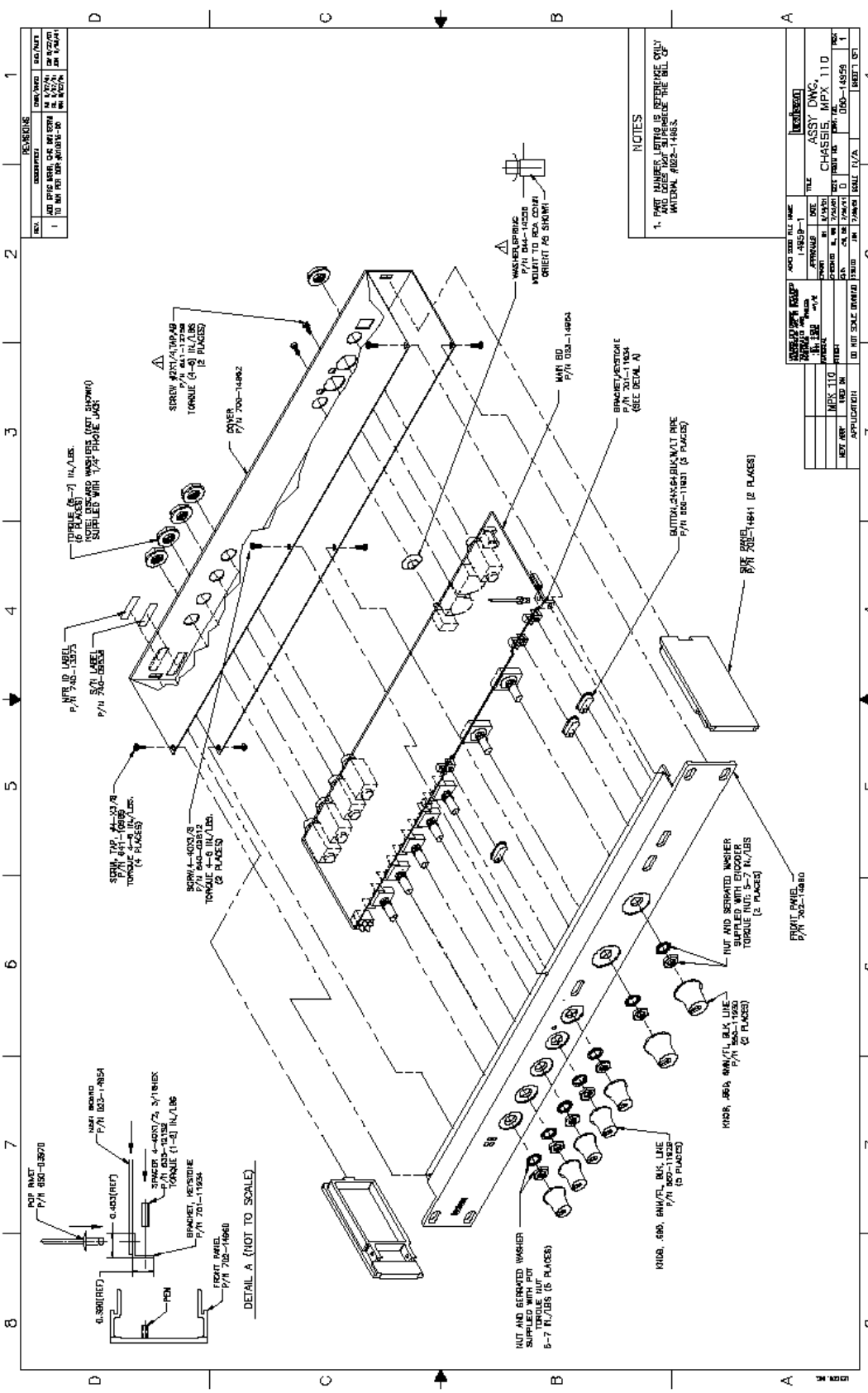
Your Notes:



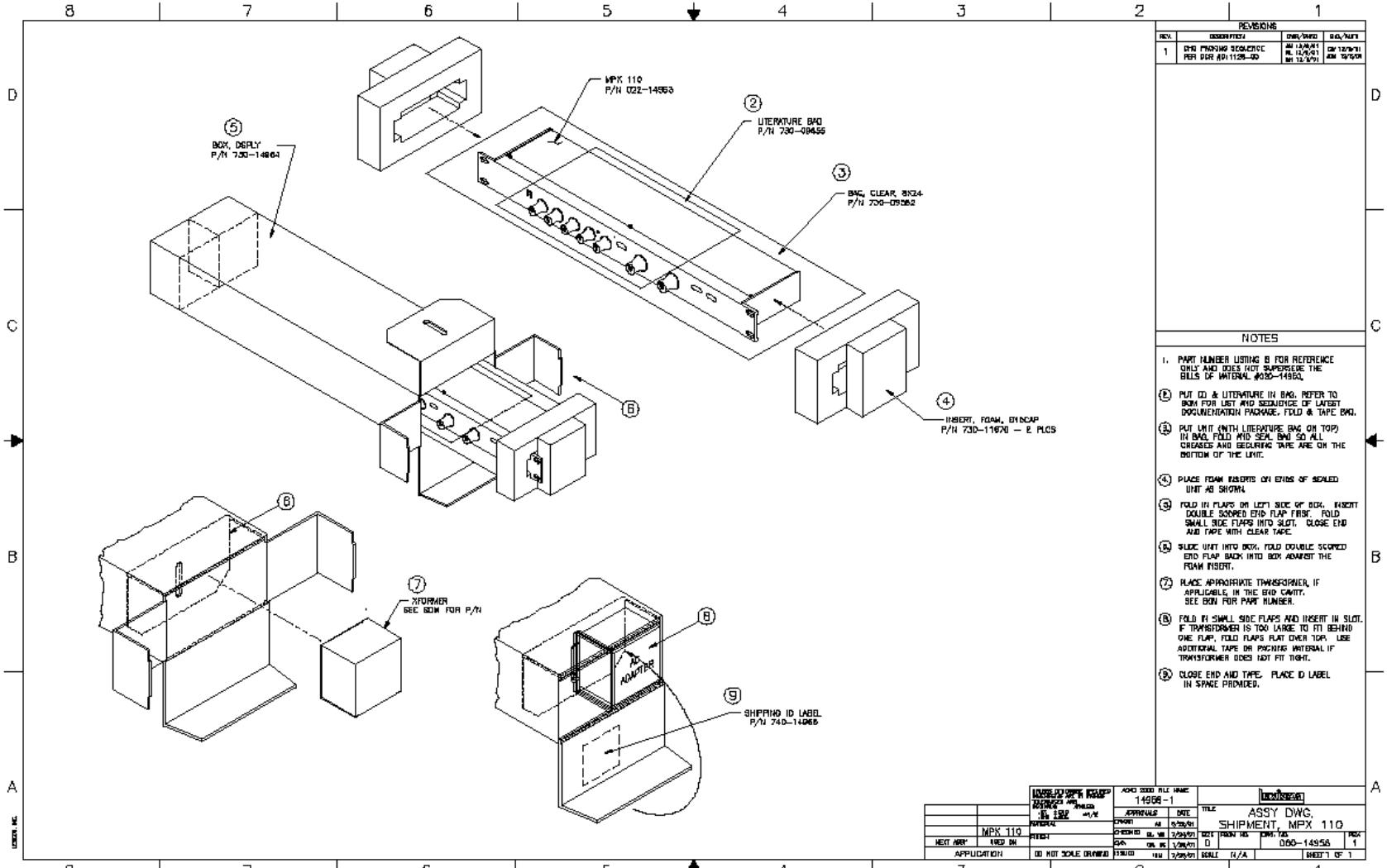
Your Notes:


lexicon
MPX110 MAIN BOARD
COMPONENT LAYOUT
2
SCALE N/A
SHEET 1 OF 1

Your Notes:


NOTES
1. PART NUMBER LISTING IS REFERENCE ONLY AND DOES NOT SUPERSEDE THE BILL OF MATERIAL #1022-14963.
ASSY DWG, CHASSIS, MPX 110
DETAIL A (NOT TO SCALE)

Your Notes:



REVISIONS			
REV.	DESCRIPTION	DWN/CHKD	ECO/APPD
1	BOM MARKING SEQUENCE PER DCR AD11128-00	AM 12/4/01 RL 12/5/01 BH 12/6/01	CM 12/6/01 ASM 12/6/01

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE THE BILLS OF MATERIAL #030-14950.
2. PUT CD & LITERATURE IN BAG. REFER TO BOM FOR LIST AND SEQUENCE OF LATEST DOCUMENTATION PACKAGE. FOLD & TAPE BAG.
3. PUT UNIT (WITH LITERATURE BAG ON TOP) IN BAG, FOLD AND SEAL BAG SO ALL CREASES AND SECURING TAPE ARE ON THE BOTTOM OF THE UNIT.
4. PLACE FOAM INSERTS ON ENDS OF SEALED UNIT AS SHOWN.
5. FOLD IN FLAPS ON LEFT SIDE OF BOX. INSERT DOUBLE SCORED END FLAP FIRST. FOLD SMALL SIDE FLAPS INTO SLOT. CLOSE END AND TAPE WITH CLEAR TAPE.
6. SLIDE UNIT INTO BOX, FOLD DOUBLE SCORED END FLAP BACK INTO BOX AGAINST THE FOAM INSERT.
7. PLACE APPROPRIATE TRANSFORMER, IF APPLICABLE, IN THE END CAVITY. SEE BOM FOR PART NUMBER.
8. FOLD IN SMALL SIDE FLAPS AND INSERT IN SLOT. IF TRANSFORMER IS TOO LARGE TO FIT BEHIND ONE FLAP, FOLD FLAPS FLAT OVER TOP. USE ADDITIONAL TAPE OR PACKING MATERIAL IF TRANSFORMER DOES NOT FIT TIGHT.
9. CLOSE END AND TAPE. PLACE ID LABEL IN SPACE PROVIDED.

		ACAD 2000 FILE NAME: 14968-1			
		APPROVALS	DATE	TITLE: ASSY DWG, SHIPMENT, MPX 110	
	MPX 110	DRAWN AS	3/29/01		
		CHECKED BL, MB	3/29/01	SIZE: D	DRAWING NO.: 060-14958
NEXT ASSY:	USED ON	QUA. DR, BS	1/28/01		REV: 1
APPLICATION	DO NOT SCALE DRAWING	ENGR. MM	3/29/01	SCALE: N/A	SHEET 1 OF 1

Your Notes:

Lexicon, Inc.
3 Oak Park
Bedford, MA 01730-1441
Tel: 781-280-0300
Customer Service Fax: 781-280-0499
Email: csupport@lexicon.com
www.lexicon.com

Lexicon Part No. 070-15026 Rev 0 Printed in U.S.A.